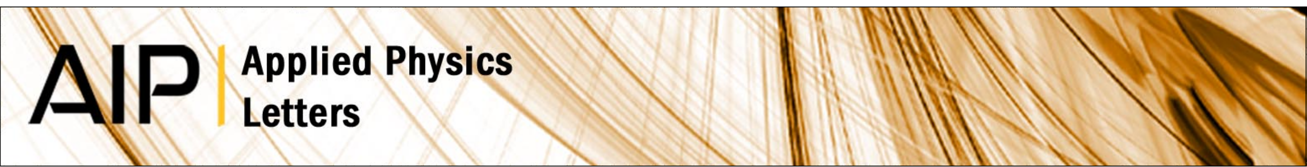

Vertically stacked individually tunable nanowire field effect transistors for low power operation with ultrahigh radio frequency linearity

Yi Song, Jun Luo, and Xiuling Li

Citation: Appl. Phys. Lett. **101**, 093509 (2012); doi: 10.1063/1.4747448
View online: http://dx.doi.org/10.1063/1.4747448
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v101/i9
Published by the American Institute of Physics.

Related Articles

Low-temperature pseudo-metal-oxide-semiconductor field-effect transistor measurements on bare silicon-on-insulator wafers
Appl. Phys. Lett. 101, 092110 (2012)

High output current in vertical polymer space-charge-limited transistor induced by self-assembled monolayer
Appl. Phys. Lett. 101, 093307 (2012)

Influence of dielectric-dependent interfacial widths on device performance in top-gate P(NDI2OD-T2) field-effect transistors
Appl. Phys. Lett. 101, 093308 (2012)

Anomalous behavior of negative bias illumination stress instability in an indium zinc oxide transistor: A cation combinatorial approach
Appl. Phys. Lett. 101, 092107 (2012)

Gate current analysis of AlGaN/GaN on silicon heterojunction transistors at the nanoscale
Appl. Phys. Lett. 101, 093505 (2012)

Additional information on Appl. Phys. Lett.

Journal Homepage: http://apl.aip.org/
Journal Information: http://apl.aip.org/about/about_the_journal
Top downloads: http://apl.aip.org/features/most_downloaded
Information for Authors: http://apl.aip.org/authors

ADVERTISEMENT

APPLIED PHYSICS LETTERS **101**, 093509 (2012)

Vertically stacked individually tunable nanowire field effect transistors for low power operation with ultrahigh radio frequency linearity

Yi Song,[1] Jun Luo,[2] and Xiuling Li[1,a)]
[1]Department of Electrical and Computer Engineering, Micro and Nanotechnology Laboratory, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801, USA
[2]Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

(Received 18 July 2012; accepted 7 August 2012; published online 30 August 2012)

In this letter, we present an experimentally feasible design of vertically stacked nanowire (NW) gate-all-around (GAA) metal-oxide-semiconductor field effect transistors (MOSFETs) for operation in radio-frequency (RF) circuits with ultrahigh linearity. We demonstrate that by properly tuning the diameters and doping levels of individual NWs in the vertical stack, a much higher third order intercept point is achieved compared to single nanowire designs, without degrading other performance metrics. This methodology for improving linearity overcomes the design tradeoff between RF linearity and power supply, and should be applicable to multi-stack nanowire GAA MOSFETs of all materials. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4747448]

For radio frequency (RF) circuits in modern communication systems, linearity is a crucial consideration for minimizing high order harmonics and inter-modulation, so as to guarantee less distortion between input and output signals. Transistor transconductance (g_m) contribution is a dominant factor for the non-linearity of RF amplifiers and other circuit elements at high frequency.[1] Unfortunately, g_m non-linearity is an inherent property of conventional transistors because of the mobility degradation at high field, as well as bias dependent source/drain (S/D) resistance[2] and channel length modulation effect (CLM).[3] High linearity is even more difficult to achieve at low power supply and room temperature, which are required for portable RF applications.

There are many reports on improving the linearity at the circuit level by integrating and individually addressing discrete devices;[4–6] however, such scheme requires more resources and larger footprint. Few efforts have been put into improving linearity at the device level. Kaya and Ma reported the approach of double-gate Si metal-oxide-semiconductor field effect transistors (MOSFETs).[7] Recently, Razavieh *et al*. demonstrated that nanowire (NW) gate-all-around (GAA) MOSFET has the potential to achieve good linearity when operating at the quantum capacitance limit.[8] These two approaches showed promising results; however, the improvements demonstrated thus far are limited in magnitude and range of operating voltage or temperature, as well as technical difficulties in realizing the full potential of these mechanisms. It is of great interests to find alternative methods to achieve high linearity using NW GAA MOSFETs, not only for their excellent digital performance[9] but also for the potential in superior analog/RF scalability.[10]

In this letter, we first provide our physical understanding of linearity in NW GAA MOSFETs. Then, we present a MOSFET device architecture that employs vertically stacked III–V NWs with tunable size and doping levels as the high mobility channel. Specifically, we use GaAs here to take advantage of its high electron mobility property. Through modeling and 3D numerical simulation, we demonstrate that by properly adjusting the doping and dimension of the stacked NWs individually, significant improvement in linearity, characterized by high IP3 at maximum transconductance point $g_{m,\max}$, can be achieved, even for low power supply operation at room temperature. Finally, we discuss other metrics for high frequency RF/Analog performance of this device architecture.

Figure 1 schematically depicts the proposed vertically stacked NW GAA MOSFET architecture, but we will analyze the g_m linearity of a single NW channel device. We adopt a charge based long channel model for g_m analysis,[11] which is valid for NW GAA MOSFETs operating at low electric field. As gate bias V_{gs} increases above threshold voltage (V_{th}) and below $V_{gs} - V_{th} < V_{ds}$ (drain bias), the transconductance of the device can be expressed by

$$g_m = \frac{2\pi\mu_{eff} R C_{ox}(V_{gs} - V_{th})}{L_{eff}}, \quad (1)$$

and when $V_{ds} = V_{gs} - V_{th}$, g_m reaches its peak value

$$g_{m,\max} = \frac{2\pi\mu_{eff} R C_{ox} V_{ds}}{L_{eff}}, \quad (2)$$

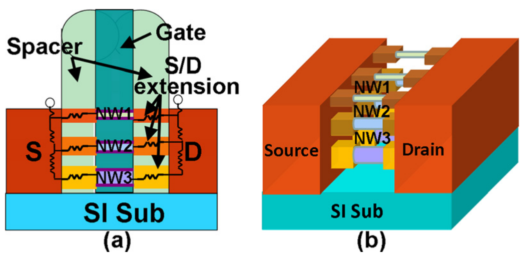

FIG. 1. Schematic illustrations of vertically stacked NW GAA MOSFET design on a semi-insulating substrate (SI Sub): (a) cross-sectional view with gate stack, S/D, and SiN spacer; (b) three-dimensional view of the stacked NWs without the gate stack.

a)Electronic mail: xiuling@illinois.edu.

 © 2012 American Institute of Physics

where μ_{eff} is the effective mobility, R is the NW radius, L_{eff} is the effective gate length which varies with CLM, C_{ox} is the gate oxide capacitance per unit area, and V_{ds} is specified as the drain-to-source bias which excludes the voltage drop across the S/D resistance. When $V_{gs} - V_{th}$ exceeds V_{ds}, both μ_{eff} and V_{ds} are reduced due to high field related mobility degradation and the impact of S/D resistance, respectively. Therefore, $g_{m,}$ which has the same expression as Eq. (2), is significantly reduced at V_{gs} beyond $g_{m,max}$.

3D numerical simulation is performed using the device simulation package synopsys TCAD SENTAURUS, employing the hydrodynamic model to incorporate non-stationary transport effects.[12] A density-gradient equation is adopted to account for the first order quantum mechanical correction.[13] The channel and S/D region material used in this design is GaAs. As an example, we assume that the NW is uniformly p-doped at low level (5e14 cm^{-3}) with a relatively large diameter ($D_{nw} = 30$ nm). The doping level in the S/D regions is high (n^+, 1e19 cm^{-3}) and the S/D extension is lower (n, 2e18 cm^{-3}). The intrinsic doping-related S/D resistance is assumed to be 2 kΩ. The NW is surrounded by 10 nm Al_2O_3 as the high–k gate dielectric and a gate metal with mid-gap workfunction of 4.5 eV (e.g., WN). A moderate value of interface charge density 5e11 $cm^{-2}eV^{-1}$ is assumed at the GaAs/Al_2O_3 interface based on published experimental data.[14] All parameters and conditions used for the simulations are for room temperature operation.

Figs. 2(a) and 2(b) show the simulated g_m vs V_{gs} curves as a function of nominal gate length L_g and drain bias V_{ds}, respectively. As L_g scales down from 800 to 100 nm, the g_m linearity becomes worse (Fig. 2(a)). This can be attributed to larger contribution of S/D resistance as well as more severe mobility degradation for devices of smaller L_g. In Fig. 2(b), it is shown that the linearity improves when V_{ds} increases from 0.1 to 0.6 V. This can be attributed to the counteraction between L_{eff}, μ_{eff}, and $V_{gs} - V_{th}$. An incremental g_m is expected when $V_{gs} - V_{th} < V_{ds}$ because g_m should increase with V_{gs} as seen in Eq. (1). However, L_{eff} increases more significantly due to CLM and μ_{eff} drops as V_{ds} increases. As a result, higher V_{ds} corresponds to a flatter g_m vs. V_{gs} curve. Therefore, as can be seen from Fig. 2, it is more challenging for NW GAA MOSFET of short channel to achieve good linearity at low V_{ds}.

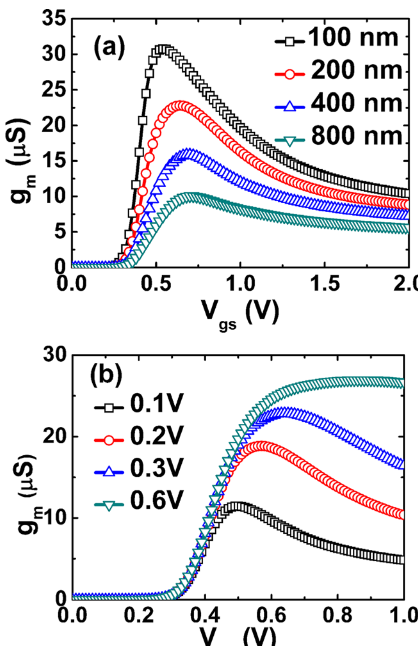

FIG. 2. Transconductance g_m as a function of gate bias V_{gs} for a single NW GAA MOSFET, with NW radius = 14 nm and p type doping concentration = 5e15 cm^{-3} (a) different L_g at $V_{ds} = 0.3$ V and (b) different V_{ds} for $L_g = 200$ nm.

Based on the analysis of single NW channel in Fig. 2, if several NW channels with different g_m vs. V_{gs} profiles, either descending or ascending within a certain range of V_{gs} bias, can be superimposed, it is possible to obtain a near constant total g_m for the NW group, thus overall better linearity. The profile of g_m vs. V_{gs} curve can be tuned by changing the NW diameter and doping concentration. Hence, we propose a vertically stacked NW GAA MOSFETs structure similar to Ref. 15 except that the stacked NW 1, 2, and 3 possess different diameters and doping concentrations, as illustrated in Figs. 1(a) and 1(b). The structure can be realized experimentally by growing the epitaxially stacked lattice-matched (e.g., GaAs/AlGaAs) or strained (e.g., InGaAs/AlGaAs) layers with different thickness and doping concentrations on top of a semi-insulating substrate, either by metalorganic vapor phase deposition (MOCVD) or molecular beam epitaxy (MBE), followed by selective etching of the sacrificial (e.g., AlGaAs) layers to form GAA structure as in Ref. 16.

From Eq. (1), the rising slope of g_m verse V_{gs} in the saturation region is $2\pi\mu RC_{ox}/L_{eff}$. V_{th} determines the position of $g_{m,max}$ and can be readily tuned by the NW doping concentration N (cm^{-3}), while it only decreases slightly with the increase of NW radius R.

We assign NW3 to be the NW with a large radius and low p type doping concentration. Thus, the NW3 channel has the lowest V_{th} and largest $g_{m,max}$, and it dominants the device performance when V_{gs} is low. Then on top of NW3, we stack NW1 and NW2 with smaller radii and heavier p type doping concentration N_1 and N_2. Therefore, these two NW channels should have relatively higher V_{th} and smaller $g_{m,max}$. The ideal situation is that the descending profile of $g_{m,R3}$ exactly compensates the rising slope of $g_{m,R1}$ and $g_{m,R2}$ throughout a wide range of V_{gs}.

Through numerical iterations, a 3-stack NW structure with N_3 (p-type, 5e15) < N_2 (p-type, 3.2e18) < N_1 (p-type, 5.8e18) and R_3 (20 nm) > R_2 (15 nm) > R_1 (8 nm) has been chosen to illustrate the methodology of the design. This representative set of parameters can keep g_m of NW1 and NW2 rise at the right V_{gs} range to compensate the descending g_m of NW3.

However, the rising slope of the g_m-V_{gs} curve is tied with the magnitude of $g_{m,max}$ as shown in Eq. (2). The magnitude of $g_{m,max}$ for smaller NWs needs to be further increased in order to effectively increase the overall g_m flatness. The local potential V_{ds} near the top surface is larger because of less voltage drop across S/D resistance, so NW1, NW2, and NW3 have to be placed from top to bottom in sequence. A spacing of 40 nm between the adjacent NWs is used for the simulation. We further adopt different S/D extension doping concentration (N_{ext1} (n-type, 1e18) > N_{ext2} (n-type, 8e17) > N_{ext3} (n-type, 5e17)) in the stack. These two design considerations lead to a larger effective V_{ds} for NW

TABLE I. Summary of design parameters and simulated electrical properties of individual and stacked NW devices at $V_{ds} = 0.3$ V.

	Radius (nm)	Doping conc. (cm^{-3})	V_{th} (V)	$g_{m,max}$ (μS)	V_{gs} @ $g_{m,max}$ (V)	IP3 @ $g_{m,max}$ (dbm)
NW1	7	p-type, 5e18	0.352	7.17	0.8	−7.50
NW2	15	p-type, 3e18	0.345	13.57	0.8	−9.59
NW3	20	p-type, 5e15	0.077	45.84	0.43	−8.86
Total	stack		0.098	47.96	0.58	−1.50

channels of smaller diameters thus result in larger $g_{m,\max R1}$ and $g_{m,\max R2}$. Table I summarizes one set of design parameters for the vertically stacked GaAs NW FET. Note that the design parameters are a function of material related data, i.e., high-field dependent mobility degradation and S/D parasitic resistance. These carefully designed parameters give rise to significantly improved linearity, i.e., g_m is nearly independent of V_{gs} over the range of 0.4–0.8 V, as shown in Fig. 3.

The significant improvement in linearity is also supported by the figure of merit for linearity, the third order intercept point (IP3), which is defined as follows:[4]

$$IP3 = \frac{2g_{m1}}{3g_{m3}R_s} = \frac{4\,\frac{\partial I_D}{\partial V_{gs}}}{R_s\,\frac{\partial^3 I_D}{\partial V_{gs}{}^3}}, \tag{3}$$

where R_s is the source resistance, g_{m1} is the transconductance, and g_{m3} is its 2nd derivative. Fig. 4 shows the calculated IP3 of the optimized vertically stacked NW GAA MOSFET compared with the individual NW cases. To reduce differentiation noise, we used cubic-spline interpolation and performed polynomial regression at 7th–9th degree. This approach generally produces smoother IP3 curves as a function of gate bias. It can be seen that IP3 is improved from −8.86 dbm (the best single wire, NW3) to −1.5 dbm (stack) at the corresponding $g_{m,max}$, which is an improvement of ∼7.36 dbm. This result represents significant advancement compared with previous efforts for device level linearity improvements both in magnitude and operating voltage range.[7,8]

It is worth noting that the improvement in linearity for the stack is bias dependent, as is the case for single NW device. One set of specific device design parameters (diameter and doping) corresponds to an optimized linearity for one specific bias range. Since the worst linearity problem is at

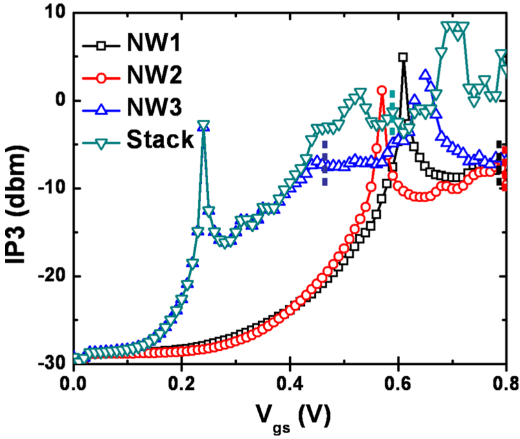

FIG. 4. Third-order intercept point IP3 (dbm) versus gate bias V_{gs} plot for NW1, NW2, NW3, and stacked NW design at $V_{ds} = 0.3$ V, the dashed vertical lines indicate the $g_{m,max}$ position.

low bias condition, our stack design example for linearity improvement was specifically optimized for low power application at V_{ds} of 0.3 V. Furthermore, as can be seen from the transfer curves shown in Fig. 5 for different gate lengths (100–600 nm), the channel length dependence of g_m linearity for stacked design is much weaker, compared to the single NW case (Fig. 2(a)). This indicates that the superposition effect of multistacked NWs for linearity improvement is valid no matter how large S/D resistance is relative to channel resistance.

For digital circuits, this stacked NW design is expected to have excellent digital performance because of the GAA structure and higher driving current density due to the stacked integration.[15] For analog circuits, there are two important metrics, one is the intrinsic gain g_m/g_d and the other is power efficiency g_m/I_d, in which g_d is the output conductance of the transistor and I_d is the drain current. Figs. 6(a) and 6(b) show the comparison of g_d and g_m/g_d, and I_d and

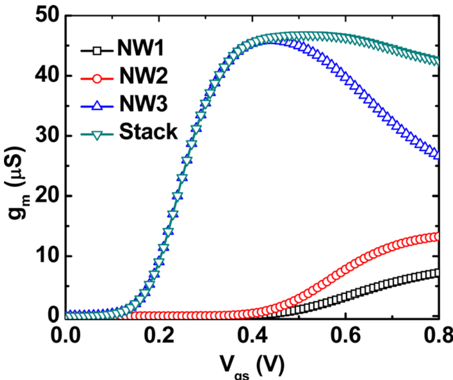

FIG. 3. Transconductance g_m verse gate bias V_{gs} plot for NW1, NW2, NW3 and the vertically stacked NWs with $L_g = 200$ nm and $V_{ds} = 0.3$ V.

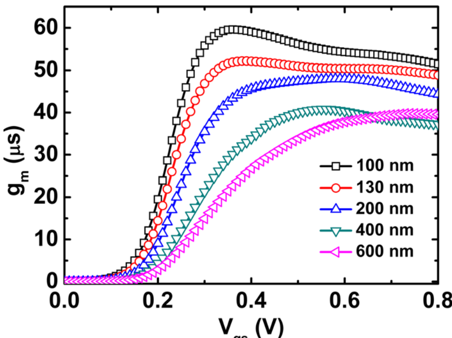

FIG. 5. Transconductance g_m as a function of gate bias V_{gs} for the stacked NW design with specified gate lengths at $V_{ds} = 0.3$ V.

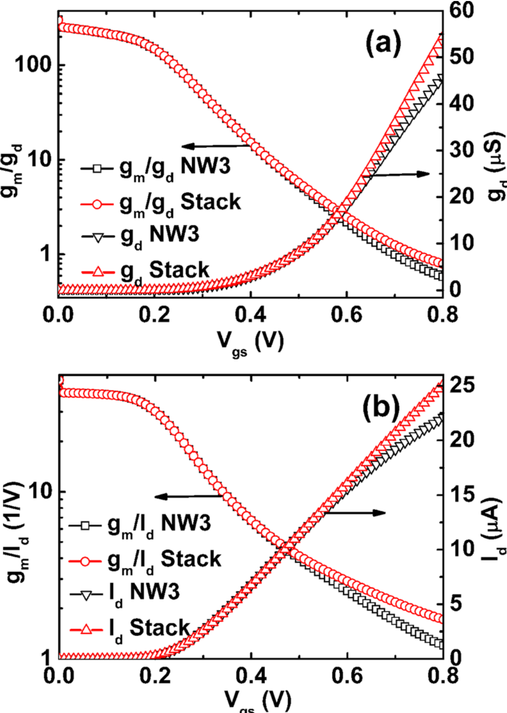

FIG. 6. (a) Self-gain g_m/g_d and (b) power efficiency g_m/I_d as a function of V_{gs} at $V_{ds} = 0.3$ V, as well as the corresponding (a) conductance g_d and (b) drive current I_d plotted on the respective right vertical axes.

g_m/I_d, respectively, as a function of V_{gs} for the stacked design and individual nanowire (NW3). We can see that both g_m/g_d and g_m/I_d of NW3 and stack design are at the same value when V_{gs} is low. However, as V_{gs} increases, g_m/g_d and g_m/I_d of the stacked case becomes larger than the NW3 case, even though g_d and I_d also increase. Thus, the vertically stacked design improves driving current without a penalty in intrinsic gain and power efficiency, which is beneficial for analog circuits.

In addition, we have compared the high frequency RF performance of the NW stack vs individual NWs, using a two-port network configuration with parasitic capacitances and intrinsic resistances included in the simulation. The cut off frequency f_T was extracted by unity current gain ($|Y_{21}/Y_{11}| = 1$ in Y-parameter matrix). The maximum oscillation frequency f_{max} was extracted by the unity mason's unilateral gain.[17] The simulation results reveal that the high frequency metrics are dominated by the largest diameter NW3 as expected because it has the largest g_m, and the stack only shows slight improvement. f_T and f_{max} start to increase sharply after V_{gs} is higher than 0.2 V. f_T of 11 GHZ and f_{max} of 140 GHZ are achieved at a low supply voltage V_{dd} of 0.3 V. All of these result indicate that the vertically stacked NW GAA MOSFET design yields a good compromise between intrinsic gain g_m/g_d, power efficiency g_m/I_d, and bandwidth f_T for low power consumption.

In summary, we have analyzed the linearity issues in NW GAA MOSFETs and presented a design of vertically stacked individually tuned NW GAA MOSFETs that can achieve excellent linearity at low bias. For a representative design, IP3 at $g_{m,max}$ reaches as high as -1.5 dbm at room temperature, with excellent high frequency RF/Analog performance. Our design offers a good solution for ultrahigh RF linearity performance and ultra-low power consumption portable system-on-chip applications. The design is experimentally feasible. The methodology should be applicable to all multi-stack NW GAA MOSFETs with different materials choice.

This work was supported by the Office of Naval Research Young Investigator Program Award N000141110634.

[1]S. Kang, B. Choi, and B. Kim, IEEE Trans. Microwave Theory Tech. **51**, 972 (2003).
[2]K. N. Parrish and D. Akinwande, Appl. Phys. Lett. **98**, 18 (2011).
[3]C. S. Ho, Y. C. Lo, Y. H. Chang, and J. J. Liou, Solid-State Electron. **50**, 1774 (2006).
[4]B. Razavi, *RF Microelectronics*, 2nd ed. (Prentice-Hall, 2010).
[5]T. W. Kim, B. Kim, and K. Lee, IEEE J. Solid-State Circuits **39**, 223 (2004).
[6]B. G. Perumana, J. H. C. Zhan, S. S. Taylor, B. R. Carlton, and J. Laskar, IEEE Trans. Microw. Theory Techn. **56**, 1218 (2008).
[7]S. Kaya and W. Ma, IEEE Electron Device Lett. **25**, 308 (2004).
[8]A. Razavieh, N. Singh, A. Paul, G. Klimeck, D. Janes, and J. Appenzeller, in *IEEE Radio Frequency Integrated Circuits Symposium*, Baltimore, MD, June 5–7, 2011.
[9]Y. Song, Q. X. Xu, J. Luo, H. J. Zhou, J. B. Niu, Q. Q. Liang, and C. Zhao, IEEE Trans. Electron. Devices **59**, 1885 (2012).
[10]S. Cho, K. R. Kim, B.-G. Park, and I. M. Kang, IEEE Trans. Electron. Devices **58**, 1388 (2011).
[11]F. Liu, J. He, L. N. Zhang, J. Zhang, J. H. Hu, C. Ma, and M. Chan, IEEE Trans. Electron. Devices **55**, 8 (2008).
[12]SENTAURUS TCAD version D-2010.03, Synopsis, Inc., Mountain View, CA.
[13]Y. M. Li, H.-M. Chou, and J.-W. Lee, IEEE Trans. Nanotechnol. **4**, 510 (2005).
[14]P. D. Ye, G. D. Wilk, B. Yang, J. Kwo, S. N. G. Chu, S. Nakahara, H. J. L. Gossmann, J. P. Mannaerts, M. Hong, K. K. Ng, and J. Bude, Appl. Phys. Lett. **83**, 180 (2003).
[15]C. Dupre, T. Ernst, V. Maffini-Alvaro, V. Delaye, J.-M. Hartmann, S. Borel, C. Vizioz, O. Faynot, G. Ghibaudo, and S. Deleonibus, Solid-State Electron. **52**, 519 (2008).
[16]J. J. Gu, Y. Q. Liu, Y. Q. Wu, R. Colby, R. G. Gordon, and P. D. Ye, Tech. Dig. - Int. Electron Devices Meet. **2011**, 769.
[17]S. Eminente, M. Alessandrini, and C. Fiegna, Solid-State Electron. **48**, 543 (2004).