III–V Junctionless Gate-All-Around Nanowire MOSFETs for High Linearity Low Power Applications

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***Abstract*— III–V junctionless gate-all-around (GAA) nanowire MOSFETs (NWFETs) are experimentally demonstrated for the first time. Source/drain resistance and thermal budget are minimized by regrowth using metalorganic chemical vapor deposition instead of implantation. The fabricated short channel (L_g = 80 nm) GaAs GAA NWFETs with extremely scaled NW width (W_{NW} = 9 nm) exhibit excellent g_m linearity at biases as low as 300 mV, characterized by the high third intercept point (2.6 dbm). The high linearity is insensitive to the bias conditions, which is favorable for low power applications.**

***Index Terms*— Linearity, nanowire, gate-all-around (GAA), GaAs MOSFET, implantation-free junctionless transistor, regrowth source/drain.**

I. Introduction

LINEARITY is one of the most important metrics for RF circuits to minimize distortion between input and output signals [1]. Most studies focus on improving linearity at the circuit level which requires a large number of devices with an enlarged footprint as well as increased power consumption [2], [3]. One solution is to adopt individual devices with high linearity. However, non-linearity is an inherent property of conventional transistors [4] and the transconductance (g_m) non-linearity is the main contribution at high frequencies [5]. For short channel devices, g_m linearity is especially degraded because of mobility degradation and severe source/drain (S/D) resistance [4], [6]. High linearity is even more difficult to achieve at low bias, which is crucial for portable RF applications. Only a few solutions have been proposed, such as operation at the quantum capacitance limit [7] and variant vertical stacking [5]. However, both of these methods require complicated growth or fabrication processes.

Junctionless (JL) FETs [8], which exploit bulk conduction, can minimize mobility degradation caused by surface roughness-related scattering or high-k surface phonon scattering [9]. The lower electric field in the channels [10] also reduced field mobility degradation when compared to traditional junction-based transistors. Ultra-thin and narrow nanowires (NWs) surrounded by multi-gate, such as using the gate-all-around (GAA) structure [11], is a critical design guideline for JL nanowire MOSFETs (NWFETs) [12]. However, scaled NWs typically suffer from parasitic S/D resistance, which can be mitigated by taking advantage of the high electron mobility and versatile bandgap and doping engineering of III-V materials [13]. Thus it is quite interesting to explore the potential for improving the linearity using III-V JL nanowire MOSFETs (NWFETs).

In this letter, we report III-V JL GAA NWFETs fabricated with an implantation-free technology through S/D regrowth by metalorganic chemical vapor deposition (MOCVD). The fabricated short channel devices (L_g = 80 nm) show excellent g_m linearity at low bias conditions (V_{dd} = 300 mV), characterized by the high third intercept point (2.6 dbm).

II. Experiments

The overall device structure and two detailed cross sectional views are illustrated in Fig. 1(a). The epitaxial layers consists of lattice-matched undoped $Al_{0.6}Ga_{0.4}As$ (100 nm) and n-type Si-doped 2×10^{17} cm^{-3} GaAs (40 nm) grown on semi-insulating (SI) GaAs (100) substrates in a MOCVD reactor. This moderate doping level was chosen to ensure the device could be effectively turned off while relatively high current could be achieved. The defined S/D areas were recessed approximately 200 nm using a 30 sec 1:8:80 H_2SO_4: H_2O_2: H_2O wet etching with a 100 nm SiO_2 hard mask. A wet-etch recess is preferred over dry-etching because it mitigates surface damage prior to regrowth. Additionally, the lateral wet-etch below the SiO_2 hard mask determines the nominal gate length. Selective area S/D regrowth of 200 nm Si-doped GaAs (5×10^{18} cm^{-3}) by MOCVD was immediately carried out. Then, $Al_{0.6}Ga_{0.4}As$/GaAs fins of 140 nm height were formed by dry etching using a new SiO_2 hard mask. The 100 nm $Al_{0.6}Ga_{0.4}As$ sacrificial layer and SiO_2 hard mask were selectively removed in 25% HF. Fig. 1(b) shows the suspended NWs which are 9 nm wide and 40 nm thick. The samples were soaked for 10 min in 10% $(NH_4)_2S$ to passivate surface and loaded into an atomic layer deposition (ALD) chamber for 9 nm Al_2O_3 as the gate dielectric, followed by 650 °C annealing for 90 s. S/D ohmic contacts were formed by evaporation of Ge/Au/Ni/Au and annealed for

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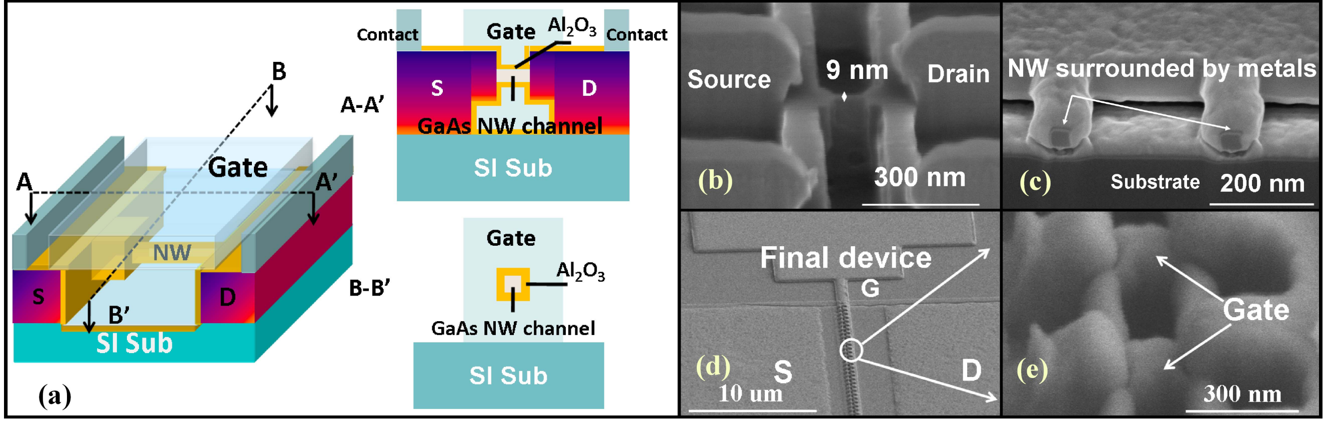

Fig. 1. (a) Schematic structure of a GaAs JL GAA NWFET on semi-insulating (SI) substrate and two cross sectional views across (AA') and parallel to (BB') S/D; (b) SEM image of suspended NWs and raised S/D; (c) FIB image of cross section of NW surrounded by gate metals; (d) Top-view SEM images of the fully fabricated JL GAA NWFET device and (e) its zoomed-in view of the gate region.

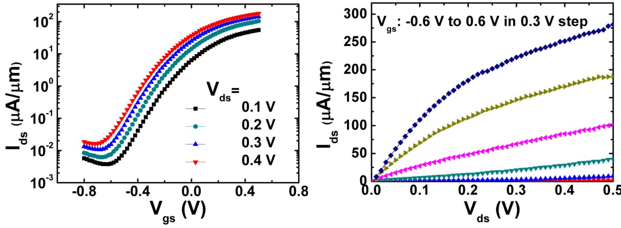

Fig. 2. (a) I_{ds}–V_{gs} and (b) I_{ds}–V_{ds} curve of a representative device with L_g = 80 nm and W_{NW} = 9 nm, H_{NW} = 40 nm.

30 s at 400 °C. Finally, Cr/Au (20 nm/200 nm) was sputtered twice, in two titled directions (45° and 135°), to ensure the gate metal fully surrounded the channel. Fig 1(c) shows a SEM imaged obtained after cross-sectional milling using Focused Ion Beam (FIB), confirming the GAA structure. Fig. 1(d) shows a SEM picture of the fully fabricated device at two different magnifications. The electrical characterization was carried out using a Keithley 4200 semiconductor network analyzer.

III. Results and Discussion

Fig. 2(a) and (b) show the measured transfer characteristics (I_{ds}–V_{gs}) and output curves (I_{ds}–V_{ds}) of a device with gate length L_g = 80 nm, NW width W_{NW} = 9 nm and height H_{NW} = 40 nm. The current is normalized by the width of the NW for this device because the operation mechanism is bulk conduction instead of surface channel conduction [14]. The extracted sub-threshold slope (SS) is 110 mV/dec, reasonable for such short channels and attributed to the good GAA electrostatic control [11]. Note that the device is biased at low voltage to explore its low power behavior and channel doping concentration is low, thus the low driving current and low transconductance (g_m) values (below). The threshold voltage (V_{th}) could be shifted more positive if a gate metal with higher workfunction is adopted.

Although the output conductance cannot be neglected because the drive current does not reach perfect saturation due to short channel effects, its value is still too low to generate significant amount of third-order current non-linearity. The output conductance non-linearity also vanishes due to the reduced output voltage swing caused by capacitive shunting effects at high frequencies [5]. Therefore we only focus on g_m non-linearity here. Fig. 3 shows the g_m vs. V_{gs} at different V_{ds} for the same device. Remarkably, the g_m is near the maximum value over a broad range of V_{gs} (0.2–0.5 V) in the linear operation region. The excellent linearity can also be verified by the third intercept point (IP3), which is the figure-of-merit commonly used to evaluate linearity performance of individual RF devices [15]. IP3 is defined as in eq. (1), where R_s = 50 Ω is system impedance for most RF systems [1], g_{m1} is the transconductance and g_{m3} is its 2nd derivative. We used cubic-spline interpolation and performed polynomial regression to smooth the IP3 curve. The inset of Fig. 3 plots the extracted IP3 as a function of V_{ds} at the V_{gs} value (0.3 V) that corresponds to the maximum g_m ($g_{m,max}$). The IP3 reaches as high as 3.8 and 2.6 dBm for V_{ds} of 0.4 and 0.3 V, respectively. These values represent significant improvement over those achieved from other approaches [7], [15]. As V_{ds} decreases, the linearity degrades only slightly to ∼ 1.5 dBm at 0.1 V, making it suitable for low bias conditions.

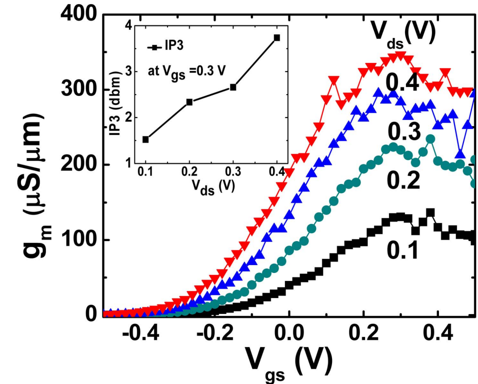

Fig. 3. gm–V_{gs} curve of a representative device with L_g = 80 nm and W_{NW} = 9 nm, H_{NW} = 40 nm. The inset shows the extracted IP3 vs V_{ds} at V_{gs} of 0.3 V.

$$IP3 = \frac{2g_{m1}}{3g_{m3}R_s} = \frac{4\frac{\partial I_D}{\partial V_{gs}}}{R_s\frac{\partial^3 I_D}{\partial V_{gs}^3}} \tag{1}$$

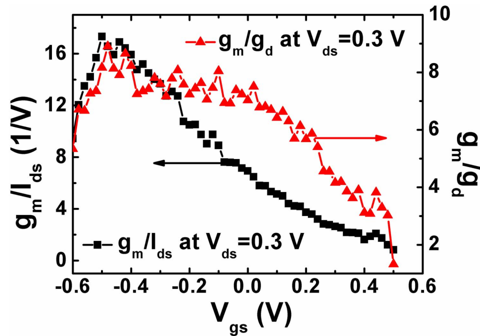

Fig. 4. Power efficiency (g_m/I_{ds}, black) and intrinsic gain (g_m/g_d, red) curves of a JL GaAs GAA NWFET with $L_g = 80$ nm and $W_{NW} = 9$ nm, $H_{nw} = 40$ nm.

The broad $g_{m,\max}$ profile is beneficial for the power efficiency g_m/I_d as shown in Fig. 4 (left axis). For a broad V_{gs} range, the intrinsic gain g_m/g_d in Fig. 4 (right axis) maintains above 4, which is comparable to other reported values [16].

The effect of device geometry W_{NW} on the linearity was also investigated. The IP3 improves from ~ -10 to 2.6 dBm when W_{NW} reduces from 60 to 9 nm for $L_g = 80$ nm. This is attributed to the higher channel resistance with decreasing W_{NW}. A higher channel resistance corresponds to less degradation of intrinsic V_{ds} when V_{gs} increases, which is beneficial for higher g_m linearity [4], especially for JL FETs.

We believe the high linearity observed is first a result of the reduced mobility degradation [14] due to the unique JL GAA structure. Unlike the uniformly doped n+n+n+ JL transistor [8], the S/D and channel doping were individually tuned in our JL NWFETs. When examining the electrostatic potential and carrier distribution along the NW cross section between our n+nn+ GAA JL and GAA inversion mode n+pn+ device by TCAD simulation (not shown here), the current conduction underneath the surface at low bias is more prevalent in the GAA JL device compared to conventional inversion mode transistor, leading to improved surface scattering, and mobility degradation. The JL transistor also has reduced electric field [10] inside the channel due to the more uniform potential profile, which mitigates mobility degradation. The reduced degradation of mobility leads to much slower drop of transconductance when gate voltage is increased [8].

The high linearity observed should also be attributed to the reduced S/D resistance, R_{SD}, which is another critical determinant for better linearity [6]. A higher R_{SD} would lower the intrinsic V_{ds} which results in worse g_m degradation as reported previously in our 3D numerical simulation results for conventional MOSFETs [4] and verified by simulation for the junctionless MOSFETs here (not shown). We have achieved R_{SD} of 304 $\Omega\,\mu$m by S/D MOCVD regrowth, which is derived from the slope of I_{ds}-V_{ds} curves with different L_g by extrapolating to $L_g = 0$. Low S/D resistance is challenging to achieve with conventional S/D implantation technology [9] due to limited activation efficiency and unrecoverable damage and associated defects to the III-V materials [17]. Our S/D regrowth technology provides the solid solubility limited doping level while eliminates the implantation damage and high temperature annealing, which should also contribute to less mobility degradation. The graded S/D extension profile depicted in Fig. 1(a) should also help to lower R_{SD}. R_{SD} can be further reduced by epitaxial regrowth of lower band gap materials such as high indium composition $In_x ga_{1-x}As$ [13].

IV. Conclusion

In summary, III-V JL GAA NWFETs have been experimentally realized for the first time by a new implantation-free S/D MOCVD regrowth process combined with GAA metal sputtering technology. The fabricated devices feature NWs as narrow as 9 nm exhibiting excellent g_m linearity with weak dependence on bias (the IP3 reaches as high as 2.6 dBm at a low bias $V_{dd} = 300$ mV). The results presented here show promise for high linearity low power RF applications.

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