# GaAs MESFET With a High-Mobility Self-Assembled Planar Nanowire Channel

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***Abstract*—We demonstrate the first metal–semiconductor field-effect transistor with a self-assembled planar ⟨110⟩ GaAs nanowire channel. Well-defined dc output and transfer characteristics have been observed with a subthreshold slope of ∼150 mV/dec, maximum $g_m$ of 23 mS/mm, and excellent on-current saturation. Bulklike mobility of $\sim 4100\ \mathrm{cm^2/V \cdot s}$ with corresponding electron concentration of $2.3 \cdot 10^{17}\ \mathrm{cm^{-3}}$ is derived by fitting the experimental data using a self-consistent long channel field effect device model.**

***Index Terms*—Charge carrier mobility, field-effect transistors (FETs), nanotechnology, semiconductor materials.**

## I. Introduction

SEMICONDUCTOR nanowires (NWs) grown with metal catalyst have received much attention over the past several years in part from the relative ease to fabricate high-quality and sophisticated 1-D nanostructures without the need for lithography and etching. NW field-effect transistors (NW-FETs) are of particular interest and have been identified as a possible route toward meeting the future logic device scaling requirements for the continuation of Moore's Law. Silicon NWs of 1 nm in diameter have already been demonstrated [1], and CMOS compatible Si/Ge materials have been used to fabricate an NW-FET with comparable performance to conventional CMOS technology [2]. III–V (e.g., GaAs, InGaAs, InSb, etc.) semiconductor materials are of great interest due to high carrier mobility and the ability to form functional heterostructures within the NW.

Recently, we have demonstrated a controlled growth method of self-aligned ⟨110⟩ GaAs planar NWs on GaAs (100) substrates with metal–organic chemical vapor deposition (MOCVD) through gold (Au) catalyzed vapor–liquid–solid mechanism [3]. Unlike conventional out-of-plane ⟨111⟩ NWs, these ⟨110⟩ planar NWs grow self-aligned in the [0–11] or [01–1] directions laterally and epitaxially on the surface and, thus, stay effectively "pinned" to the (100) substrate during growth, as shown in Fig. 1(a). They are also free of twin defects that are often found in conventional ⟨111⟩ III–V NWs. In addition, they can also be transfer printed to other substrates such as Si using a smart release scheme and standard contact printing [3]. All of these naturally make the planar NWs integratable and compatible with existing circuit design and process technology.

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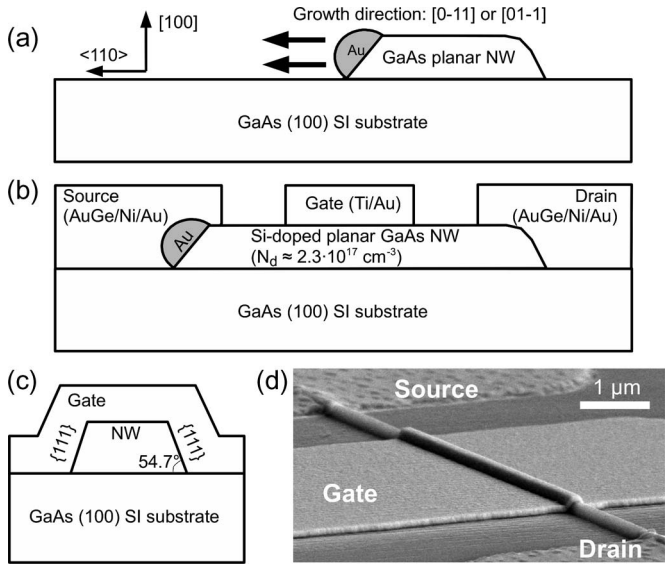


Fig. 1. (a) Illustration of planar GaAs NW growth. Planar NWs grow epitaxially and laterally on (100) substrate in the ⟨110⟩ direction. (b) and (c) Illustration of device cross section along the longitudinal and transverse directions, respectively. (d) SEM image of an NW-MESFET.

In this letter, we demonstrate a long-channel metal–semiconductor FET (MESFET) fabricated with an intentionally doped n-type planar GaAs NW channel grown on a semi-insulating (SI) GaAs (100) substrate. We discuss the dc characteristics of the device and derived intrinsic material properties. There have been a few reports of NW-MESFETs based on several different material systems, including InGaAs [4], CdS [5], ZnO [6], and GaN [7]. To the best of our knowledge, this is the first report of a bottom-up GaAs NW-MESFET.

## II. NW Growth and Device Fabrication

Planar GaAs NWs were grown using gold (Au) catalyst in an atmospheric pressure Thomas Swan MOCVD reactor. Colloidal Au nanoparticles with 250-nm nominal diameter were dispersed onto an SI GaAs (100) substrate. The substrate was then loaded into the MOCVD reactor, and GaAs planar NWs were grown at 460 °C. Trimethylgallium (TMGa) and arsine $(AsH_3)$ were used as Ga and As precursors, respectively. The NWs were intentionally doped n-type with silicon using disilane $(Si_2H_6)$ precursor. More details of the planar NW growth process can be found in [3].

Shown in Fig. 1(b)–(d) are illustrations and a SEM image of a fully processed NW-MESFET. Conventional UV-lithography was used to pattern the drain/source and gate contact regions for subsequent e-beam metal evaporation and liftoff. Ohmic

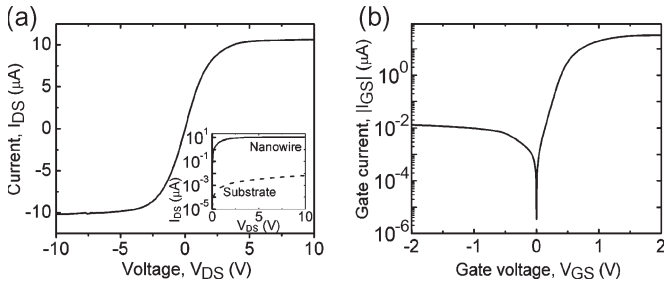


Fig. 2. (a) Two-terminal characteristics of NW-MESFET before gate deposition. (b) Schottky gate $I$–$V$ characteristics on a semilog plot.

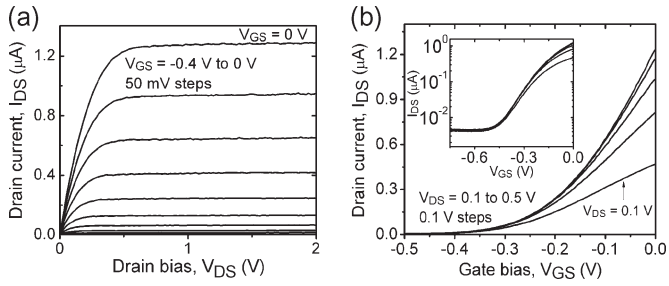


Fig. 3. Electrical characterization of NW-MESFET. (a) $I_{\rm DS}$–$V_{\rm DS}$ family of curves for $V_{\rm GS} = -0.4$ to 0 V with 50-mV steps. (b) $I_{\rm DS}$–$V_{\rm DS}$ transfer characteristics for $V_{\rm DS} = 0.1$ to 0.5 V with 100-mV steps. Inset shows $I_{\rm DS}$–$V_{\rm DS}$ plot on a semilog scale.

drain/source contacts were formed using Ge/Au/Ni/Au with annealing, while the Schottky gate contact was formed using Ti/Au metals without anneal. The cross section of the planar NW channel is trapezoidal with well-defined $\{111\}$ sidewall facets (angled 54.7° from the substrate surface) and a (100) top facet [Fig. 1(c)]. The gate then naturally formed a trigate structure with geometry and dimensions that were completely controlled during the NW growth. For ease of fabrication, the contacts and probe pads were deposited directly on the SI substrate without isolation. The device geometry examined in this letter has a gate length of 4.1 $\mu$m and a drain-to-source spacing of 7.8 $\mu$m. The dimensions of the base, top facet, and height of the trapezoidal cross section are 282, 96, and 131 nm, respectively, with little variation along the entire length of the NW.

## III. Device DC Characteristics

Shown in Fig. 2(a) is the two-terminal current–voltage ($I$–$V$) curve between the drain and source before gate deposition. The $I$–$V$ curve is linear for $|V_{\rm DS}|$ less than about 2 V indicating good ohmic contacts to the NW. However, for $|V_{\rm DS}| > 2$ V, the current is clearly saturated which is likely a result from electron velocity saturation in the NW channel. The saturation region, impacted by the scattering properties of the NW material, is typically associated more than any other region in the output characteristics with the intrinsic properties of the NW. The onset of current saturation in the NW occurs at an electric field of about 3 kV/cm which corresponds closely to the electric field required for velocity saturation in bulk GaAs [8], implying bulklike NW quality. Using the carrier concentration calculated in the next section and excluding the effect of contact resistance, the electron saturation velocity is estimated to be about $10^7$ cm/s. The leakage current (dashed line, inset of Fig. 2(a)) through the SI substrate ($\rho > 1 \times 10^7\ \Omega \cdot$ cm) is found to be negligible compared to the NW current (roughly three orders of magnitude smaller). Shown in Fig. 2(b) is the gate $I$–$V$ characteristic clearly exhibiting Schottky diode behavior. A Schottky barrier height ($\Phi_B$) of 423 mV was extracted assuming a classic thermionic emission model. This value is lower than that for a typical bulk Ti/Au/n-GaAs Schottky diode and is under further investigation.

The NW-MESFET output characteristics are shown in Fig. 3(a) where drain current ($I_{\rm DS}$) versus drain voltage ($V_{\rm DS}$) was measured at several different gate voltages ($V_{\rm GS}$). The device exhibits depletion-mode long channel characteristics with a well-defined transition from linear to pinchoff region followed by nearly constant $I_{\rm DS}$ with increasing $V_{\rm DS}$. The maximum saturation drive current is 4.6 $\mu$A/$\mu$m where we define the device width as the base dimension of the trapezoidal cross section. The transfer characteristic ($I_{\rm DS}$–$V_{\rm GS}$) of the device is shown in Fig. 3(b) for several $V_{\rm DS}$ values. The threshold voltage ($V_T$) is determined to be $-282$ mV at the drain bias $V_{\rm DS} = 100$ mV. The $I_{\rm ON}/I_{\rm OFF}$ ratio of the device is about 240 (Fig. 3(b) inset), and the subthreshold swing ($SS$) is approximately 150 mV/dec. A maximum $g_m$ of 23 mS/mm is obtained for $V_{\rm DS} = 0.5$ V.

## IV. Doping Concentration and Mobility

The NW doping concentration ($N_d$) is determined by finding the value of $N_d$ that allows for complete channel pinchoff at the threshold bias conditions. This requires the solution of Poisson's equation for the transverse cross section of the NW [i.e., the cross section in Fig. 1(c)]. Considering only ionized donor and electron concentrations, Poisson's equation can be written as

$$-\nabla^2\Phi = \frac{q}{\varepsilon_s}(N_d - n) = \frac{qN_d}{\varepsilon_s}(1 - e^{q\Phi/k_BT}) \qquad (1)$$

where $\varepsilon_s$ is the dielectric permittivity of GaAs ($\approx 13.1\varepsilon_0$), and Maxwell–Boltzmann statistics are assumed. Quantum mechanical effects can be safely neglected because of the relatively large size of the NW.

The trapezoidal cross section of the planar NW-MESFET does not allow for a simple analytical solution to (1) and instead we use the finite element method for a numerical solution. To determine $N_d$, the boundary condition at the side and top facets of the NW are set as $V_{\rm bound} = -V_{\rm bi} + V_T - V_{\rm DS}$, where $V_{\rm bi}$ is the built-in voltage, and $V_{\rm DS}$ is the drain bias used to extract $V_T$ ($V_{\rm DS} = 0.1$ V and $V_T = -0.282$ V in this case). $V_{\rm bi}$ is equal to $\Phi_B = 423$ mV minus the term $(k_BT/q)\ln[N_d/N_c]$ where $N_c$ is the effective conduction band density of states. As an approximation, the SI substrate was treated as an ideal insulator and a vanishing electric field normal to the interface was assumed. Using these boundary conditions and iterating until a suitable solution was found, the doping concentration was determined to be $N_d = 2.3 \cdot 10^{17}\text{cm}^{-3}$.

To determine the low-field electron mobility ($\mu_n$), the NW-MESFET was modeled with a standard long-channel MESFET analysis generalized for an arbitrary NW cross-sectional geometry. The active gated portion of the NW-MESFET can be modeled using the gradual channel approximation which is valid for a long-channel device. The ungated NW portion

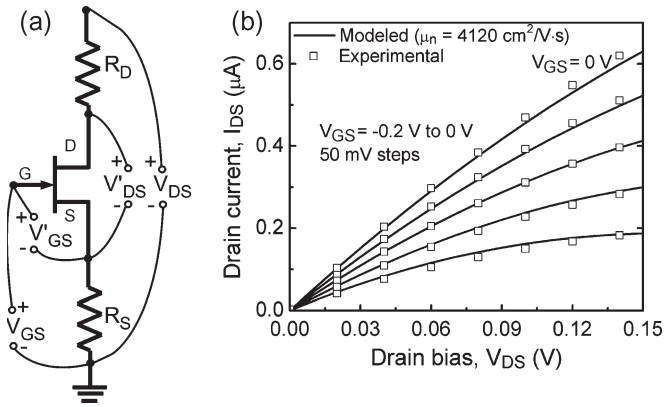


Fig. 4. (a) Equivalent circuit for an NW-MESFET that is used to model the device $I$–$V$ characteristics in the linear regime. (b) Modeled and experimental $I_{\rm DS}$–$V_{\rm DS}$ family of curves in the linear regime. The modeled data were calculated using $\mu_n = 4120\ \text{cm}^2/\text{V}\cdot\text{s}$.

existing between the source/drain and the ends of gate contacts needs to be included in the model as series resistance to accurately extract $\mu_n$ [9]. The equivalent circuit for the NW-MESFET is shown in Fig. 4(a), where $V'_{\rm GS}$ and $V'_{\rm DS}$ represent the reduced potentials in the gated portion

$$V'_{\rm GS} = V_{\rm GS} - R_S I_{\rm DS} \tag{2}$$
$$V'_{\rm DS} = V_{\rm DS} - I_{\rm DS}(R_D + R_S) \tag{3}$$

and $R_S$ and $R_D$ are the source and drain series resistances. $R_S = 38\ \text{k}\Omega$ and $R_D = 40\ \text{k}\Omega$ are determined from the resistance per unit length ($R_l = 23.5\ \text{k}\Omega/\mu\text{m}$) of the ungated NW portion, extracted from the two-terminal $I$–$V$ data in Fig. 2(a). The drain/source contact resistance was not measured directly but is implicit in $R_l$ and thus lumped into $R_S$ and $R_D$. However, this leads to an underestimation of the contact resistance and, therefore, a more conservative estimate of $\mu_n$. In the linear regime of operation, the current ($I_{\rm CH}$) at any point ($x$) in the gated portion of the NW-MESFET channel is

$$|I_{\rm CH}(x)| = qN_d\mu_n A\,(V'_{\rm GS}, V_x)\,\frac{dV_x(x)}{dx} \tag{4}$$

where $V_x(x)$ is the channel potential, and $A(V'_{\rm GS}, V_x)$ is the generalized cross-sectional area of the *undepleted* conducting region of the channel and is a function of both $V'_{\rm GS}$ and $V_x$. Assuming current is constant along the channel, the drain current ($I_{\rm DS}$) of the device can be determined by integration

$$I_{\rm DS} = (qN_d\mu_n/L) \int_{V_x(0)=0}^{V_x(L)=V'_{\rm DS}} A\,(V'_{\rm GS}, V_x)\,dV_x \tag{5}$$

where $L$ is the gated channel length. The integral in (5) can be numerically evaluated for a particular value of $V'_{\rm GS}$ by solving (1) to calculate and sum the values of $A(V'_{\rm GS}, V_x)$ for incremental values of $V_x$ between $V_x = 0$ and $V_x = V'_{\rm DS}$. Equation (5) can then be solved in a self-consistent manner with (2) and (3) such that the current is equivalent through both the gated and ungated device regions.

The mobility was extracted by using $\mu_n$ as a fitting parameter to fit (5) to experimental $I_{\rm DS}$–$V_{\rm DS}$ curves. With this approach, we extract $\mu_n = 4120\ \text{cm}^2/\text{V}\cdot\text{s}$. This value corresponds closely with reported values of electron mobility in bulk GaAs with a doping density of $N_d \approx 2\cdot 10^{17}\ \text{cm}^{-3}$ [10]. This is indicative of the excellent material quality of the planar GaAs NWs. Shown in Fig. 4(b) are calculated $I_{\rm DS}$–$V_{\rm DS}$ curves solved from (5) with $\mu_n = 4120\ \text{cm}^2/\text{V}\cdot\text{s}$ in the linear regime of device operation, which shows excellent agreement with the experimental data. The doping concentration and mobility extracted from all devices tested range between $N_d = 1.9\cdot 10^{17} - 4.4\cdot 10^{17}\ \text{cm}^{-3}$ and $\mu_n = 3000 - 4540\ \text{cm}^2/\text{V}\cdot\text{s}$, consistent with bulk GaAs values.

## V. Conclusion

In conclusion, we have reported the first GaAs MESFET fabricated with a self-assembled planar NW channel. The material quality of such NW channel is manifested in its bulklike electron mobility. We expect that with smaller diameter NWs, short-channel self-aligned process, higher mobility lower bandgap III–V NWs such as InAs, as well as suitable gate oxide [11], [12], NW-FETs using the planar ⟨110⟩ NWs as channels can achieve significantly enhanced transfer characteristics. Considering the planar, self-aligned, and transferable nature [3], this type of NW-FETs hold the promise to a bottom-up approach for high-performance III–V FETs for next-generation integrated circuit applications.

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