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Sub-100 nm Si nanowire and nano-sheet array formation by MacEtch using a non-lithographic InAs nanowire mask

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Abstract
We report a non-lithographical method for the fabrication of ultra-thin silicon (Si) nanowire (NW) and nano-sheet arrays through metal-assisted-chemical-etching (MacEtch) with gold (Au). The mask used for metal patterning is a vertical InAs NW array grown on a Si substrate via catalyst-free, strain-induced, one-dimensional heteroepitaxy. Depending on the Au evaporation angle, the shape and size of the InAs NWs are transferred to Si by Au-MacEtch as is (NWs) or in its projection (nano-sheets). The Si NWs formed have diameters in the range of ∼25–95 nm, and aspect ratios as high as 250 in only 5 min etch time. The formation process is entirely free of organic chemicals, ensuring pristine Au–Si interfaces, which is one of the most critical requirements for high yield and reproducible MacEtch.

(Some figures may appear in colour only in the online journal)

1. Introduction

In recent years, silicon (Si) nanowires have shown unique properties that could lead to significant breakthroughs in conventional electrical, optical, and energy harvesting and storage devices [1–4]. For example, high aspect ratio Si nanowires could enhance the energy capacity and lengthen the life cycle of lithium batteries [1]; radial p–n junctions in nanowires increase the carrier collection efficiency of a photovoltaic device [2]; nanowire arrays on a surface increase light trapping from the solar spectrum [5]; thermal conductivity of Si nanowires smaller than ∼50 nm in diameter is predicted to be significantly lower than that of bulk Si while the electrical conductivity and Seebeck coefficient are not greatly effected, leading to applications in thermoelectric devices [3, 6]. For these reasons, the formation of very thin and high aspect ratio Si nanowire arrays has been researched extensively in recent years [7–11].

To produce high aspect ratio Si nanowire arrays, either a bottom-up (i.e. growth) [9] or top-down (i.e. lithography and etching) [10] approach can be used. The most commonly used bottom-up approach can provide very thin Si nanowires by tuning the size of the metal catalysts using the vapor–liquid–solid (VLS) growth method. For example, a Si nanowire array with an average diameter of 39 nm has been grown using 20 nm size of Au colloids and the aspect ratio of nanowires reached 100 [9]. However, metal catalyzed VLS growth results in the incorporation of metal impurities in the nanowires, which potentially create deep levels in the bandgap and degrade device performances [12]. One of the top-down approaches, metal assisted chemical etch (MacEtch), a wet but directional etching method, has been widely used to generate Si nanowires recently [13–15]. The MacEtch solution consists of a mixture of an oxidizing agent and an acid. The most commonly used combination for MacEtch of Si is hydrofluoric acid (HF) and hydrogen peroxide (H_2O_2). The oxidizing agent (i.e. H_2O_2) generates free holes (h^+) catalyzed by the metal (e.g. Au), which is not consumed. These holes oxidize Si at the metal–semiconductor interface and HF removes the oxidized silicon to solution. Under controlled conditions, etching only takes place in metal covered areas, so that an array of Si nanowires can be produced when a metal mesh pattern is used [13, 14]. The aspect ratio of the nanowire produced is essentially limited

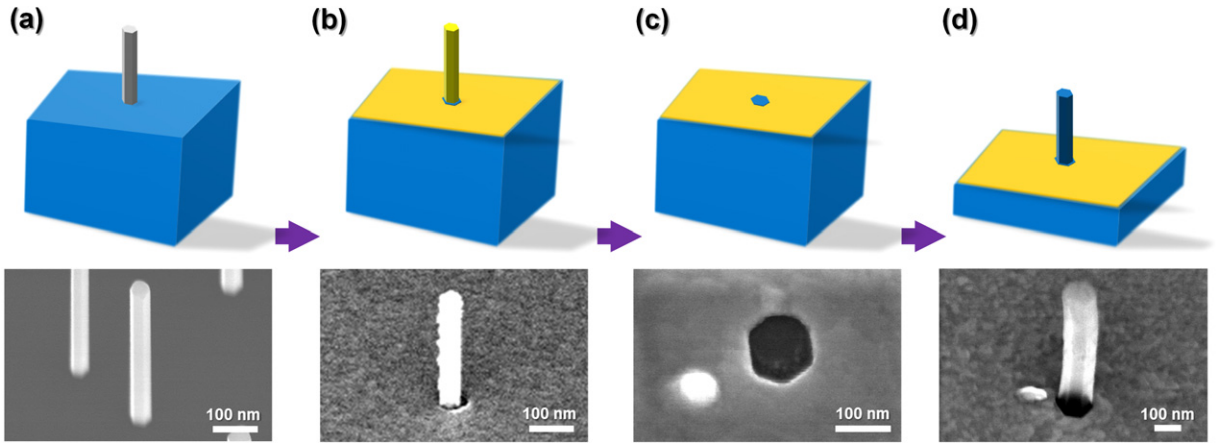

Figure 1. Illustration of the process sequence to form the Si nanowire array and the corresponding SEM image at each stage: (a) grow InAs nanowires on a Si(111) substrate; (b) deposit a thin Au film on the InAs nanowire mask; (c) selectively remove the InAs nanowires in piranha solution; and (d) form Si nanowires by MacEtch.

by etching time, because etching takes place only directly underneath the metal catalysts under controlled conditions. MacEtch is presumably free of surface damage compared to dry etching because no high energy ions are involved in the process. Moreover, MacEtch does not cause metal contamination compared to VLS growth. MacEtch takes place at room temperature, thus the metal catalysts cannot be incorporated in the core of the Si nanowires and the metal at the surface can be readily removed by chemical solutions. To perform MacEtch, lithography techniques are commonly used to produce a mask for the generation of metal patterns on a semiconductor (e.g. Si) surface. Several methods have been used to produce sub-100 nm feature sizes including nanoimprint [16], block-copolymer [17], or e-beam lithography [18]. However, these lithography methods use organic masks such as PMMA, SU-8, or photoresists [10, 11], which often stain the semiconductor surface by forming hydrocarbons. This can inhibit MacEtch if the semiconductor and metal interface is not pristine. We have recently demonstrated wafer-scale, self-assembled InAs nanowire growth on Si(111) substrates [19]. Here we report an organic chemical free method to reliably produce sub-100 nm diameter Si nanowire as well as nano-sheet arrays by utilizing these InAs nanowires as a mask for metal catalyst patterning in MacEtch of Si.

2. Experimental details

For the growth of the InAs nanowire mask, a metal organic chemical vapor deposition (MOCVD) system (A200/4, Aixtron inc.) was used [19]. A Si(111) wafer (p-type, $\rho =$ 0.15–0.25 Ω cm) was etched in a buffered oxide etch (BOE) solution for 10 min to remove native oxide on the surface. After that, the wafer was rinsed with deionized (DI) water and dried with a N_2 gun. Then, the sample was immediately loaded into the MOCVD chamber. The growth chamber was pumped down to 100 mbar and heated to the growth temperature (i.e. 520–570 °C) under hydrogen (H_2) flow. Trimethylindium [$(CH_3)_3In$, TMIn] and arsine (AsH_3) were simultaneously switched into the reactor. The molar flows of TMIn and AsH_3 were 6.7×10^{-6} and 4.91×10^{-4} mol min^{-1}, respectively. TMIn was shut off at the end of nanowire growth but AsH_3 flow was maintained until the reactor was cooled down to 270 °C. InAs growth preferentially occurs along the [111] direction. Thin InAs nanowire with diameters that are adjustable in the range of ∼25–95 nm can be grown on Si(111) substrates.

For MacEtch, 20 nm thick Au film was first evaporated on the InAs nanowire sample using an E-beam evaporator, followed by the removal of the InAs nanowires selectively from the Si substrate by etching in piranha solution (i.e. H_2SO_4:H_2O_2) for 10 min with sonication. An Au mesh pattern is thus formed with the mesh size defined by the InAs nanowire diameter. The volume ratio of the MacEtch solution used for producing vertical Si nanowires was 5, 1, and 1 for concentrated HF, H_2O_2, and EtOH, respectively. The ratio of H_2O_2 had to be increased for producing the slanted Si nanowire array. The typical etching rate was ∼3 μm min^{-1}. After MacEtch, the Si nanowire sample was rinsed in methanol and dried on a hotplate (70 °C) to prevent clumping or breaking of the nanowires. The morphology of nanowires was characterized by SEM (Hitachi-S4800).

3. Results and discussion

The fabrication process of the sub-100 nm thin Si nanowire arrays is illustrated schematically along with SEM images in figure 1. In step (a), vertical InAs nanowires are grown on a Si(111) substrate. The self-assembled InAs nanowires are grown in the [111] direction and have six $\{1\bar{1}0\}$ side facets [19]. This is followed by step (b): the deposition of an Au film on the InAs nanowire mask sample. In step (c), InAs nanowires are completely removed chemically and a holey Au pattern is left on the Si surface. The hole is hexagonal which is identical to the InAs nanowire cross section. It is worth noting that 100% liftoff rate with clean cut edges is

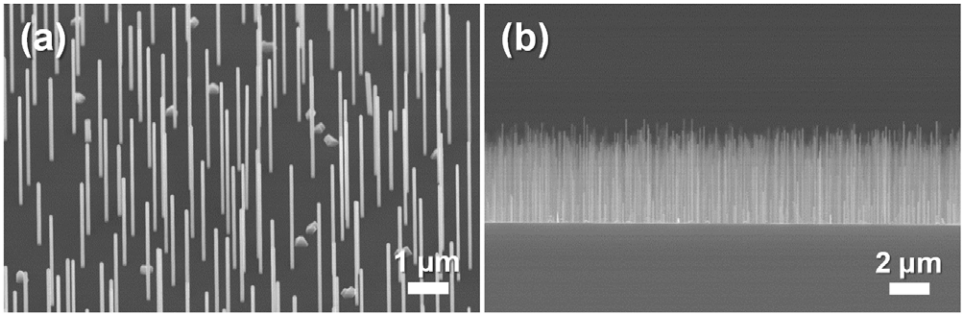

Figure 2. A heteroepitaxially grown vertical InAs nanowire array on a Si(111) substrate: (a) 45° tilted and (b) side-view SEM images.

achieved consistently for feature sizes this small (<100 nm) due to the high aspect ratio of the InAs nanowires. In step (d), the metal catalyst descends into Si by removing Si directly underneath, leaving behind Si nanowires by MacEtch. Detailed experimental conditions that are used to produce the corresponding SEM images are described in the experimental part.

An example of vertical InAs nanowires grown on a Si(111) substrate is shown in figure 2. In severely lattice mismatched systems (e.g. InAs on Si), the strain energy of the adlayer can be lowered by forming isolated islands. Under proper growth conditions, these islands preferentially elongate to the [111] direction rather than increase their sizes. Therefore, a InAs nanowire array can be grown on a Si surface regardless of the wafer size or number of wafers in the reactor. The average diameter and density of the InAs nanowire array are very uniform with below 5% variation across a 2″ wafer in our experiment. Although site control is not feasible because of the self-assembly nature, the diameter and density of the InAs nanowire array can be tuned by growth parameters such as temperature and V/III ratio. The density of InAs nanowire array can be controlled in a range of $\sim 1 \times 10^8$–5×10^9 cm^{-2}. Detailed growth parameters for the growth of InAs NW arrays can be found in our previous publication [19].

Figures 3(a)–(c) are SEM images of the InAs nanowires grown at three different temperatures. Increasing growth temperature promotes the migration of the adatom mobility on the Si surface during growth, causing the formation of larger diameter nanowires [19]. The controllability over InAs NW diameters allows the formation of Si nanowires with different diameters. InAs nanowires grown at 520, 540, and 570 °C are 30 ± 10, 60 ± 10, and 85 ± 10 nm in diameter, respectively. The diameter distribution, measured over a 10×10 μm^2 area, is plotted in figure 3(d). Note that the growth time for the nanowire mask was 5 min, resulting in 4 μm long InAs nanowires, although the total growth time including heating and cooling time is about 1 h. Importantly, total consumption of the TMIn and AsH_3 sources was only 0.005 and 0.7 g, respectively, for the growth of a InAs nanowire array on a 2 inch Si wafer.

Figure 4(a) shows an optical image of a $\sim 2 \times 2$ cm^2 area of Si nanowire array produced by MacEtch. Figures 4(b) and (c) are the 45° tilted and side-view SEM images, respectively, for the sample in (a). Figures 4(e)–(g) show the Si nanowires produced from three masks with different InAs nanowire diameters (~30, 60, and 90 nm). The average diameter of the Si nanowire array is the same as that of the InAs nanowire mask. The density of the nanowire array is $\sim 1.5 \times 10^8$ cm^{-2} inferred by the InAs nanowire density on the mask. Remarkably, the height of the vertical Si nanowires is ~15 μm and the aspect ratio reaches ~250 (figure 4(c)) after 5 min etch time. To our knowledge, this is the highest aspect ratio sub-100 nm Si nanowire array ever reported. The MacEtch concentration and etch rate have been optimized to eliminate porosity [11] and generate vertical and solid Si nanowires in this case. Further MacEtch of the sample causes the Si nanowires to clump up at the top when dried due to surface tension, as shown in figure 4(d). By varying the concentration of the MacEtch solution, a slanted Si nanowire array can also be formed (figure 4(h)) [11]. The slanted geometry can be useful in increasing the contact area between metal and nanowire tip for better device performance [20].

In addition to the nanowire geometry, unique to a high aspect ratio metal patterning mask, ultra-thin vertical Si nano-sheets can also be generated. Figures 5(a)–(c) illustrate the process sequence to generate Si nano-sheets. By angled evaporation and the shadowing effect of the nanowires, Au metal patterns consisting of thin slit openings can be formed. The widths of the slits correspond to the InAs nanowire widths and lengths are defined by the InAs nanowire projections in the Si substrate plane, which are determined by the evaporation angle and nanowire heights. Shown in figure 5(d) is an SEM image of Si nano-sheets generated from 40 s Au-MacEtch by evaporating Au on the InAs nanowire mask with the sample tilted by ~30° angle. The height and length of the resulting Si nano-sheets are ~2 and ~1 μm, respectively, but the thickness is only ~60 nm. Note that the edge roughness of such narrow slits is minimal since the InAs nanowire diameter is extremely uniform and sidewalls are smooth. For example, the diameter variation of a 30 nm diameter nanowire is only ±1 nm along the nanowire height, confirmed by TEM analysis. The edge roughness of the thin slit pattern generated by such a nanowire mask is comparable to that of the state-of-the-art nanoimprint pattern [21]. The ultra-thin vertical Si nano-sheets can be used for fundamental studies of two-dimensional electron or thermal transport, as well as other applications.

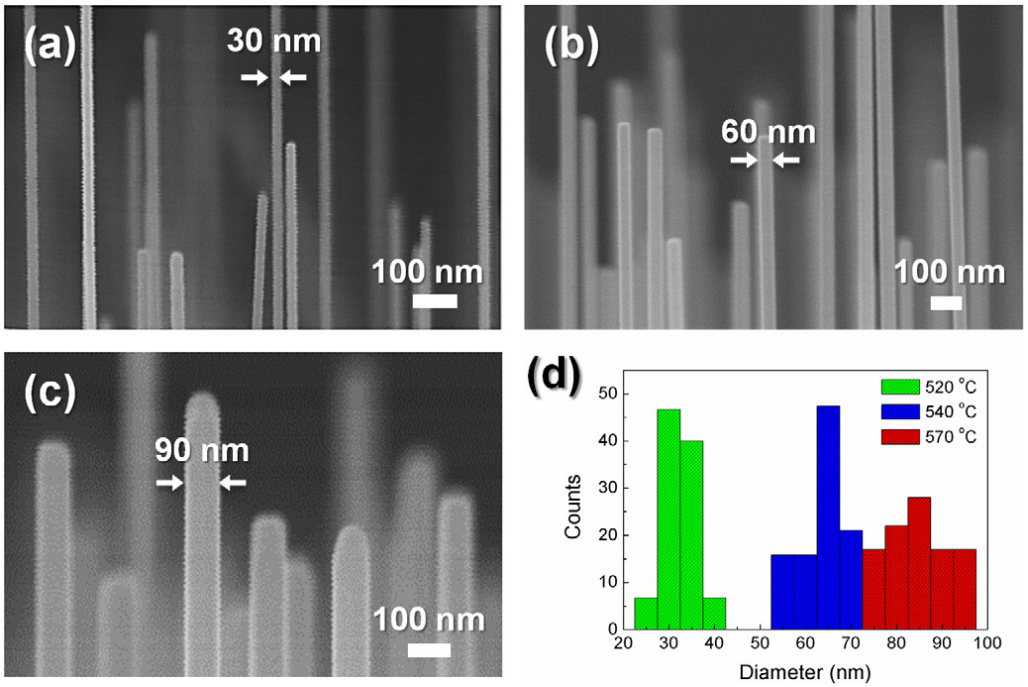

Figure 3. Side-view SEM images of InAs nanowires grown at (a) 520, (b) 540, and (c) 570 °C. (d) Diameter distribution of the nanowires at different growth temperature. The average diameter of the nanowire array increases with growth temperature.

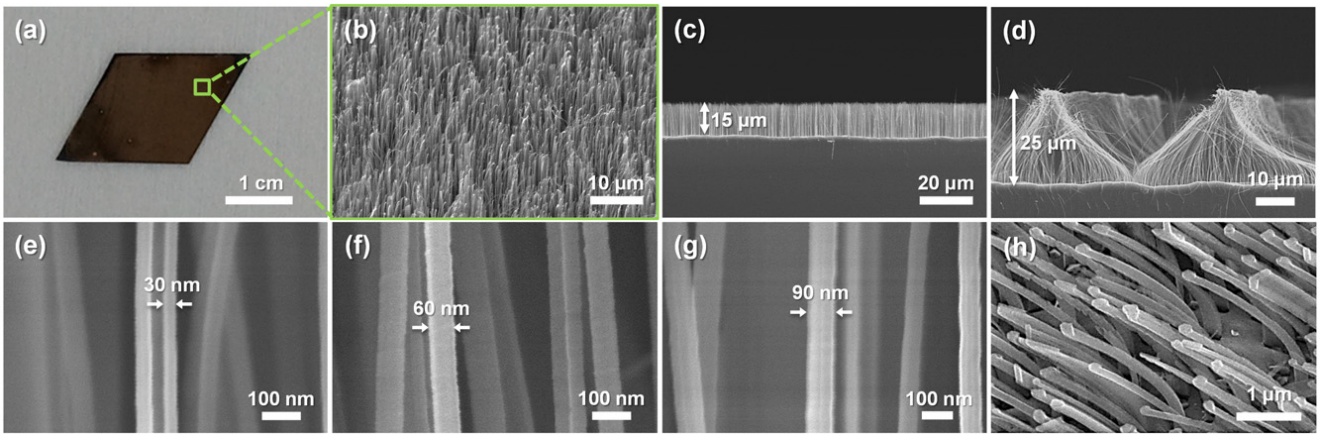

Figure 4. MacEtch produced Si nanowire arrays using a InAs nanowire mask. (a) Optical image of the Si nanowire array on a 2 × 2 cm^2 wafer piece. (b) 45° tilted, and (c) side-view SEM image for the sample in (a). (d) Si nanowires bundled together at the top. (e)–(g) Fabricated Si nanowires with different diameters. (h) Slanted Si nanowire array.

4. Conclusions

In summary, Si nanowire and nano-sheet arrays with sub-100 nm width are formed by MacEtch using a novel non-lithographical InAs nanowire mask. Relying on the chemical selectivity of heterogeneous inorganic materials (InAs versus Si in this case), the method reported here is inherently free from organics and thus from potential contamination that affects metal patterning yield and reproducibility. The InAs NW mask is cost-effective, high throughput, and scalable. The high aspect ratio nature of the nanowire mask allows the generation of not only nanowires, but also laterally elongated ultra-thin nanostructures through shadow evaporation. With further site and density control of the InAs nanowire mask, ordered, high density, high aspect ratio ultra-thin Si nanowires and nano-sheets can be formed efficiently at a wafer-scale. The high aspect ratio Si nanowires and nano-sheets could be applicable to batteries, photovoltaics, thermoelectric devices, and 3D transistors.

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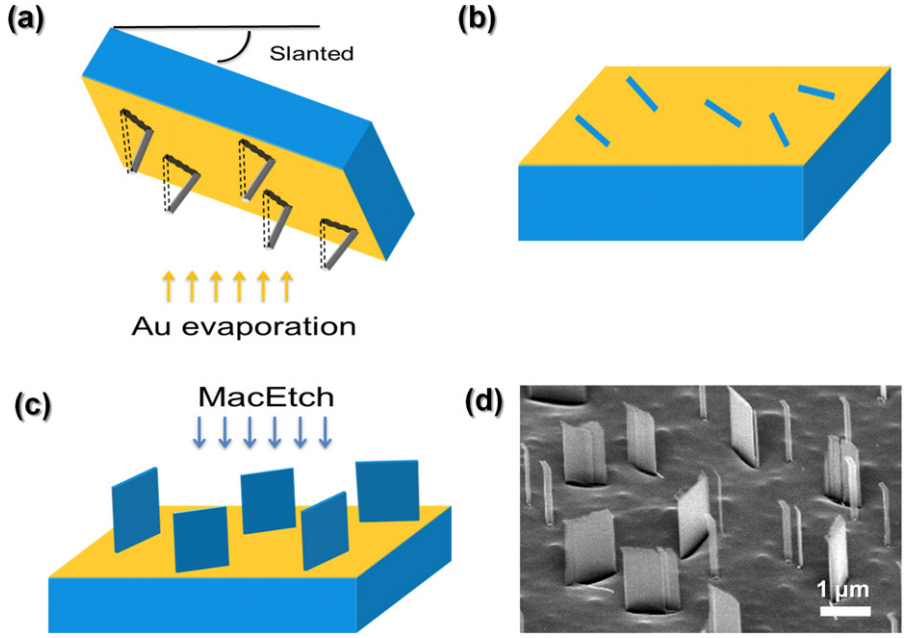

Figure 5. Illustration (a)–(c) of the process sequence to form vertical Si nano-sheets: (a) angle evaporation of Au onto a tilted Si wafer shadowed by InAs nanowires. The dashed lines are there to guide the eyes to the InAs nanowire projection; (b) selectively etch away InAs nanowires in piranha solution to form the Au pattern with slit openings, where the slit width and length are defined by the nanowire width and evaporation angle; (c) transfer the Au slit pattern to Si by MacEtch to form Si nano-sheets. (d) SEM image of ultra-thin Si sheets after 40 s etching (height:length:thickness = 2 μm:1 μm:$\sim$0.06 μm). Note that the nanowire-like structures in between the nano-sheets probably originate from metal patterns formed over small islands among the tall InAs nanowires on the Si wafer.

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