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Planar GaAs Nanowires on GaAs (100) Substrates: Self-Aligned, Nearly Twin-Defect Free, and Transfer-Printable

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ABSTRACT

We report the controlled growth of planar GaAs semiconductor nanowires on (100) GaAs substrates using atmospheric pressure metalorganic chemical vapor deposition with Au as catalyst. These nanowires with uniform diameters are self-aligned in <110> direction in the plane of (100). The dependence of planar nanowire morphology and growth rate as a function of growth temperature provides insights into the growth mechanism and identified an ideal growth window of 470 ± 10 °C for the formation of such planar geometry. Transmission electron microscopy images reveal clear epitaxial relationship with the substrate along the nanowire axial direction, and the reduction of twinning defect density by about 3 orders of magnitude compared to <111> III−V semiconductor nanowires. In addition, using the concept of sacrificial layers and elevation of Au catalyst modulated by growth condition, we demonstrate for the first time a large area direct transfer process for nanowires formed by a bottom-up approach that can maintain both the position and alignment. The planar geometry and extremely low level of crystal imperfection along with the transferability could potentially lead to highly integrated III−V nanoelectronic and nanophotonic devices on silicon and flexible substrates.

Semiconductor nanowires have been extensively studied in the past decade for applications in nanoelectronics and nanophotonics. The bottom-up approach through metal-catalyzed growth allows for the routine synthesis of nanometer-scale devices and the flexibility to form functional heterostructures with materials that are otherwise incompatible as thin films. To date, many classes of photonic and electronic devices have been demonstrated including electrically pumped lasers, light-emitting diodes, photodetectors, field effect transistors, and logic gates.[1−3] III−V semiconductor nanowires are of particular interest because of their direct bandgap, high carrier mobility, and ability to form heterojunctions. However, the abundance of twin-plane defects has been widely reported,[4,5] which degrade the optical and electronic properties. Wafer-scale integration with current planar processing technology remains a challenge for the commonly grown out-of-plane nanowire geometry.[3,6] Ex situ assembly methods are required to transfer and coarsely align the nanowires in plane on a functional device substrate, but without control of the position of individual nanowires on a wafer scale.[7−11] More traditional top-down methods have alternatively been successfully used to transfer semiconductor micro/nano wires to dissimilar substrates.[12,13]

The most widely reported process of semiconductor nanowire growth is the vapor−liquid−solid (VLS)[14] or the recently discovered vapor−solid−solid (VSS)[15,16] mechanism. The driving force for crystallization is the supersaturation of liquid or solid alloy droplets which are formed by metal catalytic absorption of gas reactants. The diameters of the nanowires are determined by the size of the seed particles, while the growth direction has largely been reported to depend on the surface free energy.[17] It has been shown for III−V materials with a cubic lattice that the lowest free energy surface is (111)B and thus nanowires grown on (111)B substrates are vertically aligned and perpendicular to the substrate.[18] When (100) substrates are used, most nanowires still grow in the <111>B direction, which is 35.3° angled from the substrate.[18] Other growth directions have been observed sporadically during nanowire growth, presumably due to modification of free energy by strain, surface tension etc.,[17,19−24] and such nanowires have reportedly shown fewer twinning defects.[17] Promising results of planar <110> GaAs nanowire growth has been shown previously; however the length of the nanowires was limited to about 500 nm (before the growth direction changed) and control of the yield of planar nanowires through modulation of growth conditions was not addressed.[20] Recently, the self-

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alignment of horizontal ZnO nanowires on an a-plane sapphire substrate using phase transport process through the control of catalyst size and spacing[22,25] has been reported.

In this research letter, we report a method that enables controlled large area growth of self-aligned planar <110> GaAs nanowires on GaAs (100) substrates using metalorganic chemical vapor deposition (MOCVD). As confirmed by transmission electron microscopy (TEM), the nanowires have a zinc-blende crystal lattice and are mostly free of twin-plane defects for nanowires as long as 6 μm. A systematic growth study shows that the morphology and yield of the planar nanowires can be controlled primarily through the growth temperature. In addition, by growing the planar nanowires on a sacrificial layer we demonstrate the possibility of parallel transfer of the highly aligned planar nanowires to a foreign substrate. The nanowires discussed in this letter were grown with a Thomas Swan atmospheric pressure MOCVD reactor. Trimethylgallium (TMGa) and arsine (AsH_3) were used as the gallium and arsenic precursors, respectively. Typical AsH_3 flow was 200−500 sccm and TMGa was at 10 sccm (36−90 V/III molar ratio). GaAs (100) substrates were degreased and subsequently treated with diluted hydrochloric acid (HCl) to remove the native oxide. Colloidal gold (Au) nanoparticles with 5−20 nm nominal diameters were then directly deposited on the substrate (the substrates were not treated with an adhesion layer such as poly-L-lysine). After colloidal gold deposition, the samples were transported to the MOCVD reactor and annealed at 620 °C under AsH_3 flow for 10 min. This step served to alloy the Au with the GaAs substrate and desorb any residual native oxide. The temperature was ramped down to the growth temperature (420−520 °C) and TMGa was subsequently introduced into the reactor. After the growth, samples were cooled under AsH_3 flow. Nanowire length and morphology were analyzed with a Hitachi 4800 scanning electron microscope (SEM) at 15 kV.

Shown in Figures 1a−c are SEM images of as grown GaAs nanowires catalyzed using Au nanoparticles at 460−475 °C under the conditions described above. The nanowires are self-aligned in plane in either the [1-10] or [-110] direction (Figure 1c) axially, and the radial cross-section appears to be in a half-cylindrical shape. Nanowires that are 30 nm or smaller in diameter exhibit smooth sidewall morphology. Few larger nanowires as large as 500 nm in diameter are also observed and probably resulted from the aggregation of Au nanoparticles during dispersion and annealing steps. The large ones display distinct crystal facets on the wire sidewalls but the orientation is still in-plane along the two <110> directions.

Planar <110> nanowires almost completely disappear at lower temperatures (Figure 2a) and are replaced by mostly angled <111> nanowires. In contrast, at higher growth temperatures (Figure 2b), well-aligned in-plane triangular shapes (appear like “school of tadpoles”) are observed with the apex of each triangle terminated with a Au nanoparticle. The top surface of the triangular wire is (001) while the sidewall facets of the triangles appear to be {111}. The lengths of these triangular planar wires are noticeably shorter

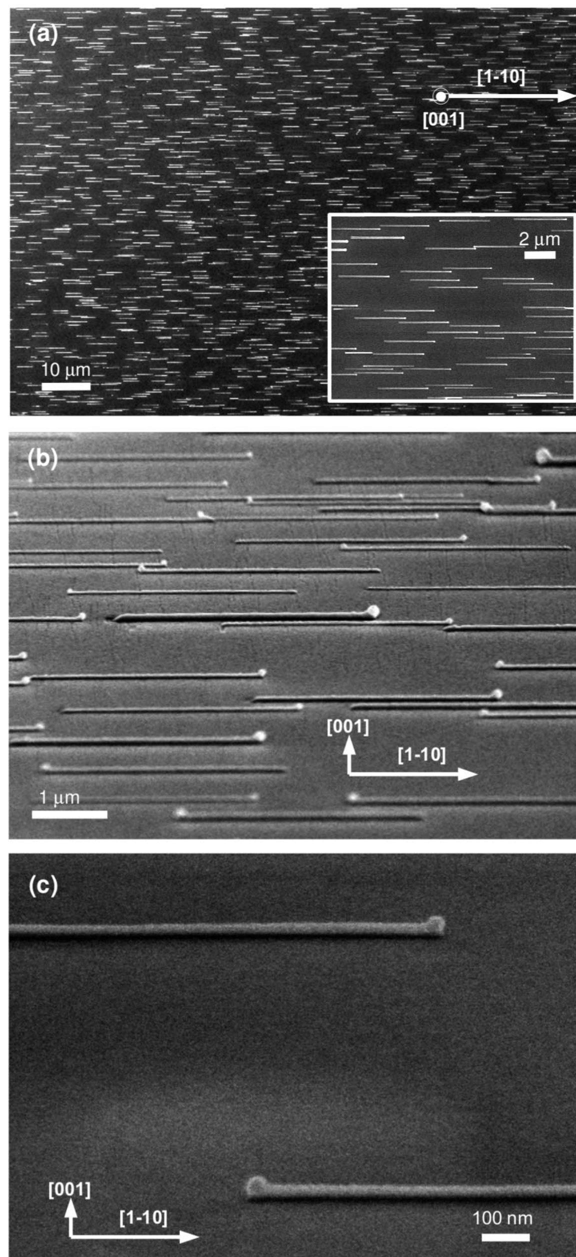

Figure 1. Planar <110> GaAs nanowires grown on GaAs (100) substrate. (a) Low, (b) medium, and (c) high magnification SEM images of well-aligned <110> planar nanowires. Nanowires were grown at 460 °C in (a,b) and at 475 °C in (c). Sample is not tilted in (a) and tilted 75° in (b,c).

than those cylindrical planar nanowires at 460 °C. We attribute the shape of these triangular wires to the simultaneous growth along the Au-catalyzed VLS nanowire growth direction <110>, and the temperature enhanced nanowire sidewall growth. The sidewall growth apparently suppresses the VLS growth, leading to lower axial growth rate. This is analogous to the tapered vertical nanowire growth on (111)B substrates, where a wider base in contact with the substrate and narrower top were formed at elevated temperatures and longer growth time.[26]

Clearly, temperature, a well-controllable growth parameter, can be modulated to change the nanowire growth direction. Shown in Figure 3 is an Arrhenius plot of the planar axial

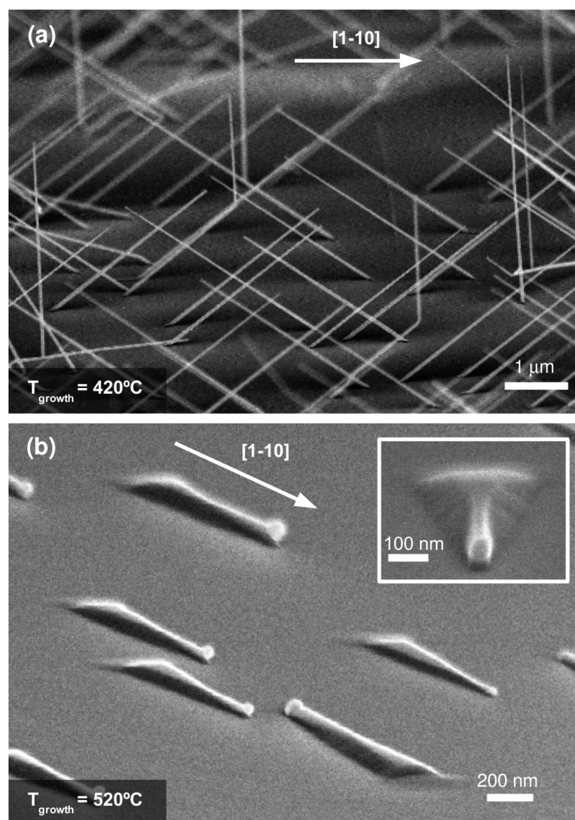

Figure 2. GaAs nanowires grown on GaAs (100) substrate. The nanowire orientation and morphology is controlled primarily through modulation of the growth temperature. SEM images show (a) predominantly <111> nanowires grown at 420 °C and (b) tapered, well-aligned <110> planar nanowires grown at 520 °C. Inset of panel b shows high-magnification SEM image of tapered planar nanowire as viewed along its growth axis (scale bar is 100 nm). Sample is tilted 75° in both images.

nanowire growth rate as a function of growth temperature. It can be seen that the growth rate increases with temperature initially then reaches a plateau before falling. Interestingly, the Arrhenius plot for <110> planar nanowire growth rate resembles that for the MOCVD grown vertical GaAs <111> nanowires reported previously using the same metalorganic precursor,[27] both qualitatively and in extracted activation energy. As pointed out by the previous report,[27] the activation energy for VLS nanowire growth is approximately the same as that for bulk epitaxial growth on (100) GaAs substrate with no catalyst, and the onset of the plateau corresponds to the complete pyrolysis temperature of the metalorganic precursor TMGa.[28] This indicates that VLS growth is hindered by the cracking efficiency of TMGa below the peak temperature, and thus increases with temperature. At higher temperatures, nanowire VLS axial growth competes with nanowire sidewall growth, resulting in a decreased growth rate with increasing temperature. The optimum growth window for <110> planar nanowires with uniform diameters is in the region where the axial growth rate is the highest. 470 ± 10 °C has been identified as the optimum temperature window as indicated in Figure 3 under the specified growth conditions described above. As high as 95% yield of planar <110> nanowires with uniform diameter has been achieved.

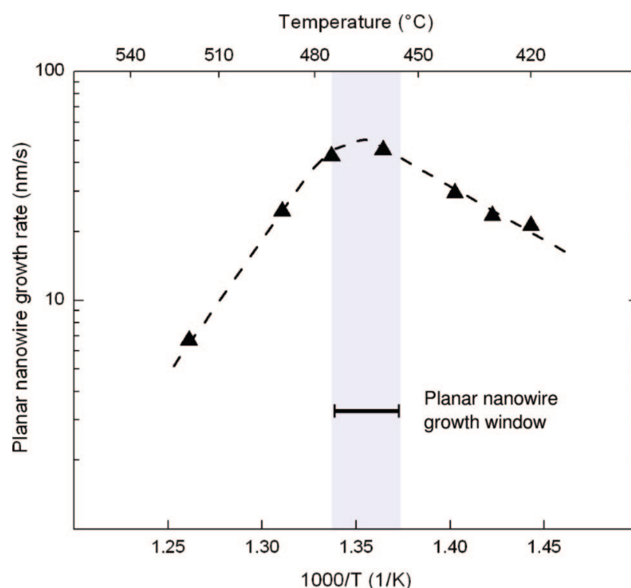

Figure 3. Planar GaAs nanowire growth rate. Arrhenius plot with the shaded region corresponding to the ideal temperature range for planar nanowire growth. All data points were obtained with equivalent growth conditions (excluding temperature) and 2 min growth times. Dashed line is a guide for the eyes.

We have observed spacing between adjacent <110> planar nanowires as small as 15 nm which suggests the possibility of a high density of planar nanowires. Occasionally, a planar nanowire will spontaneously change growth direction and merge with an adjacent planar nanowire (typically less than 50 nm away). The merging nanowire will then grow on top or side-by-side to the adjacent nanowire to form a single larger nanowire (see Supporting Information for examples) while maintaining planarity. In areas of very high Au nanoparticle density, the yield of <111> directed nanowires typically increases. Given that we commonly observe closely spaced planar nanowires as described above, the increased density of <111> nanowires is most likely due to the lack of surface area for the <110> planar nanowires to nucleate and grow. Through proper patterning of catalyst, we expect that <111> nanowires can be avoided.

TEM observations were carried out on a JEOL 2010 microscope with a LaB_6 filament. Cross-sectional TEM specimens were prepared by gluing two films face-to-face using M-bond, followed by standard mechanical grinding down to 20 μm and ion milling down to perforation. Elemental analysis using energy dispersive X-ray spectroscopy (EDS) was conducted with a JEOL 2010F equipped with an Oxford EDS detector. Shown in Figure 4a is a TEM image of a planar GaAs nanowire terminated by an Au particle. Along the axis of the nanowire, mostly limited to regions less than 0.5 μm from the Au-GaAs interface, there is a periodic deviation in the nanowire diameter of approximately ± 2.5 nm. Periodic instability of nanowire diameter has been reported for nonplanar nanowires and is attributed to a feedback mechanism in the supersaturation of the catalyst.[29] Figure 4b shows a high resolution TEM image obtained from the interface between the GaAs planar nanowire and the (100) GaAs substrate as viewed along a

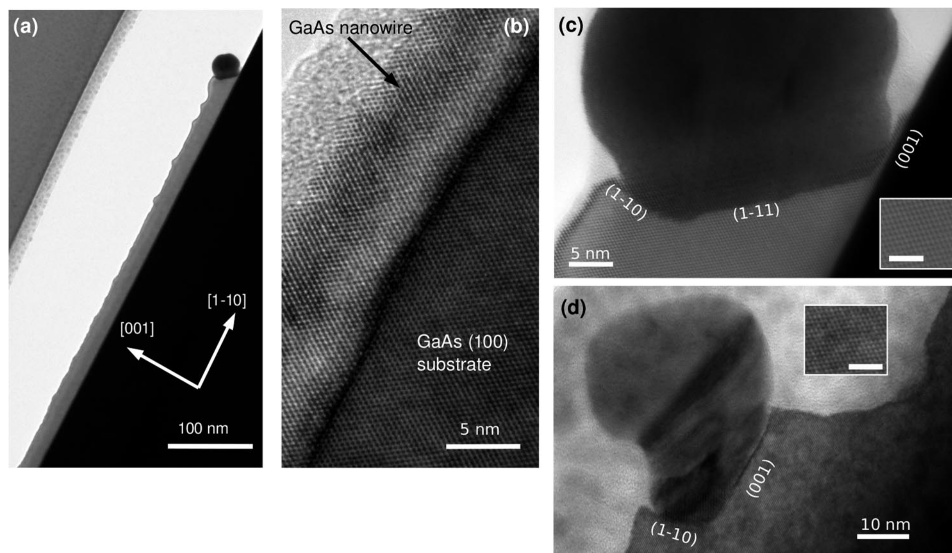

Figure 4. TEM images of planar GaAs nanowires. (a) Low-magnification TEM image of <110> planar nanowire without stacking faults. (b) High-resolution TEM image of the nanowire-substrate interface. The top half of the nanowire delaminated during sample preparation and is not visible. The contrast at the nanowire-substrate interface is most likely from a thickness difference between the two regions. (c,d) TEM images of the two types of Au-GaAs interfaces observed. Insets show defect-free zinc-blende lattice (scale bars are both 2.5 nm).

<110> direction that is perpendicular to the nanowire growth direction. The GaAs nanowire clearly extends the substrate zinc-blende lattice epitaxially and the growth direction is along the <110> direction. No apparent misfit dislocations and only a few stacking faults have been found for the 5 μm long nanowires examined, in contrast to the high density of twin boundaries (~5−10 nm in average spacing) reported in GaAs <111> nanowires.[4,30,31] This is an improvement of twin defect density by about 3 orders of magnitude. Unlike the <111> nanowires, the interface between the Au and GaAs for these planar <110> nanowires is not perpendicular to the growth direction. As shown in Figure 4c, the Au nanoparticle intercepts with GaAs at (001) and (110) facets, in addition, a well-defined (111) interface (35° angled from the growth direction) between Au nanoparticle and GaAs is actually formed. Observations of (111) interface between metal catalyst nanoparticle and semiconductor have been reported previously for non-<111> nanowires, presumably due to its low interfacial energy. We have also observed another type of Au−GaAs interface, as shown in Figure 4d, where the Au nanoparticle deformed to form mainly (110) and (001) interfaces with Au elevated on top of the long (001) facet. The composition analysis by EDS of Au particles indicates a Ga composition of 5% or less. This is consistent with continued precipitation of Ga out of the Au/Ga alloy to form GaAs due to the presence of AsH_3 overpressure during cooling down,[15] which could result in different Au-GaAs interfaces due to the high mobility of Au particles.

It has been reported that the surface free energy could be modified depending on nanowire density, and size (thus edge tension), substrate type and Au/Ga eutectic composition.[23,32−35] Although we did not study the nanowire size effect systematically, we do not believe the formation of <110> planar nanowire on (100) substrate is size related because we have observed planar wires as small as 20 nm and as large as 500 nm in diameter. Close examination of the nanowire initial growth region clearly shows an angled sidewall profile (not shown), implying <111> as the onset nucleation direction. The dominant planar geometry for the tapered nanowires (Figure 2b) suggests that sidewall growth promotes planar growth. Furthermore, a two step growth experiment, where initial growth was carried out at 460 °C followed by continued growth at 420 °C, yielded <110> planar nanowires. This confirms the critical role of the energetics of the initial nucleation in determining the nanowire growth direction. We hypothesize that planar nanowire growth initiates in the angled <111> direction via VLS mechanism, but becomes quickly (likely within a few monolayers) pinned to the (100) substrate due to growth from the acute angle sidewall; planar growth subsequently proceeds by the Au catalyzed VLS mechanism.

As indicated by the TEM results, the planar nanowires are epitaxially attached to the substrate. For certain applications, it is desirable to have the nanowires detached from the growth substrate and transferred to a foreign substrate such as silicon or flexible polymer. For out-of-plane nanowires, this is typically done by sonicating the nanowires from the growth substrate into a solution followed by dispersion onto a foreign substrate. However, achieving both the controlled positioning and alignment of transferred nanowires on a wafer scale has not been demonstrated. In our case, transfer of planar nanowires can be achieved by growing the nanowires on a sacrificial layer epitaxially deposited on the substrate; the nanowires can then be released from the substrate (while maintaining their position and alignment) by selectively removing the sacrificial layer. Thus we can exploit the as-grown alignment along the <110> direction and control the position of nanowires through patterned catalyst. The released nanowires can then be transferred to a foreign substrate. For GaAs materials, the most commonly used sacrificial layer $Al_xGa_{1-x}As$ ($x \geq 0.5$) is easily oxidized in air and cannot be used as the surface for Au catalyst

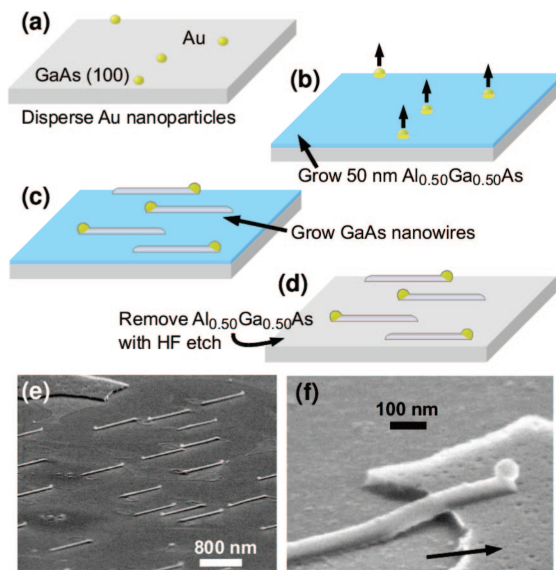

Figure 5. Schematic (a−d) of the process used to release planar GaAs nanowires from the growth substrate: (a) Au catalyst is dispersed on GaAs (100) substrate. (b) A thin (25−50 nm) sacrificial $Al_{0.50}Ga_{0.50}As$ epilayer (blue colored) is grown at $T = 625$ °C; Au catalyst elevates above the sacrificial layer and onto the surface. (c) GaAs nanowires are grown at $T = 460$ °C. (d) GaAs nanowires are released when $Al_{0.50}Ga_{0.50}As$ sacrificial layer (blue colored) is removed with HF. (e) SEM image of released GaAs nanowires. The nanowires clearly remain aligned. (f) SEM image of a nanowire that is partially released from the substrate (arrow points to the remaining sacrificial layer).

deposition for subsequent planar nanowire growth. Instead, we have developed a method to grow the sacrificial layer after the Au nanoparticles are deposited, which is schematically illustrated in Figure 5a−d. Au nanoparticles were first deposited on the GaAs substrate (Figure 5a), which was then annealed as described above. A thin (25−50 nm) sacrificial $Al_{0.50}Ga_{0.50}As$ epilayer was grown at 625 °C to favor noncatalyzed overgrowth on the substrate. The Au nanoparticles were elevated under such growth condition above the sacrificial layer and onto the surface (Figure 5b). The temperature was then ramped down to 460 °C to favor Au-catalyzed growth and planar GaAs nanowires were grown on the $Al_{0.50}Ga_{0.50}As$ epilayer (Figure 5c). The samples were cooled under AsH_3 flow and removed from the MOCVD reactor. To release the GaAs nanowires from the substrate, the $Al_{0.50}Ga_{0.50}As$ epilayer was wet etched and removed with aqueous HF (49% HF) (Figure 5d). Figure 5e,f shows the result of such a process after the sacrificial layer ($Al_{0.50}Ga_{0.50}As$) is etched with HF to release the GaAs nanowires. The alignment of the nanowires clearly does not change when they are released from the substrate.

The morphology and structural properties of GaAs nanowires grown on $Al_{0.50}Ga_{0.50}As$ behaves identically to GaAs nanowires directly grown on a GaAs substrate. Using TEM, we have confirmed that GaAs nanowires grown on an $Al_{0.50}Ga_{0.50}As$ sacrificial layer also have an extremely low level of twin defects (see Supporting Information). Considering the epitaxial relationship between the planar GaAs nanowire and growth substrate (see Figure 4b), this observation is consistent with the negligible lattice constant mismatch (0.07%) between GaAs and $Al_{0.50}Ga_{0.50}As$. In addition, the growth rates of GaAs nanowires grown on the sacrificial layer ($Al_{0.50}Ga_{0.50}As$) and directly on GaAs substrate are nearly equivalent. However, for higher aluminum composition $Al_xGa_{1-x}As$ layer, reduced nanowire growth rate (Au-catalyzed) is observed due to the competing overgrowth on highly reactive $Al_xGa_{1-x}As$ ($x > \sim0.55$) surface. The overgrowth also prevents clean release of nanowires in subsequent steps, making $Al_xGa_{1-x}As$ ($x > 0.5$) not suitable as sacrificial layers in this case.

After the nanowires are released, they can readily be lift-off and transfer-printed to desired substrates. Using a similar process developed by other groups for the transfer of carbon nanotubes,[36,37] we have successfully transferred the GaAs nanowires from their native growth substrate to a silicon (100) substrate with the process illustrated in Figure 6a−d. We first release GaAs nanowires from the growth substrate using the procedure described in Figure 5 and then evaporate a 100 nm of Au onto the released nanowires (Figure 6a). Using thermal release tape (REVALPHA, Nitto Denko) that is mounted on a poly(dimethylsiloxane) (PDMS) stamp, the Au layer together with the nanowires are then peeled off the growth substrate (Figure 6b). Evaporated Au adheres poorly to the GaAs substrate surface, however the bond between the Au layer and released nanowires is strong enough such that the nanowires remain attached to the Au layer during this step. The Au layer with nanowires is then transferred to a bare silicon substrate and the entire assembly is heated to 120 °C (Figure 6c). This heating will cause the thermal tape to lose its adhesion to the Au layer. The Au with nanowires will then remain on the silicon surface after the PDMS stamp and thermal tape are removed from the silicon (Figure 6d). Finally, the Au is removed with a 20 s KI/I_2 (Transene) wet etch thus revealing the aligned nanowires on the silicon surface. Figure 6e,f shows a SEM image of planar GaAs nanowires that have been transferred to a silicon substrate. Most of the nanowires have clearly maintained their alignment throughout the entire transfer process. The discoloration of the silicon surface and nanowires evident in Figure 6e,f is from the Au etchant which tends to leave behind a scum that is difficult to rinse away. Although here we demonstrate the transfer of planar nanowires to silicon, the same process can be used to transfer the nanowires to any substrate that can withstand a 120 °C bake and Au wet etch. To the best of our knowledge, this is the first demonstration of a large area direct transfer process for nanowires formed by a bottom-up approach that can control both the position and alignment. Future work includes patterning the catalyst and controlling the growth direction ([-110] or [1-10]) such that highly aligned arrays of position-controlled nanowires can be transferred.

In conclusion, self-aligned planar <110> GaAs nanowires grown by atmospheric pressure MOCVD on GaAs (100) substrates have been reported. The growth modes between planar and angled nanowires can be modulated by growth temperature. The temperature window for the planar nanowire formation is ∼20 °C at the experimental condition specified. The reported research could potentially lead to

large scale integration with existing microelectronics due to the planar geometry and rejuvenate nanowire related optoelectronic research due to the extremely low level of crystal imperfection. The possibility of transferring the self-aligned planar nanowires to other substrates while maintaining both the position and alignment has been demonstrated which could enable flexible electronics and photonics at a true nanometer scale.

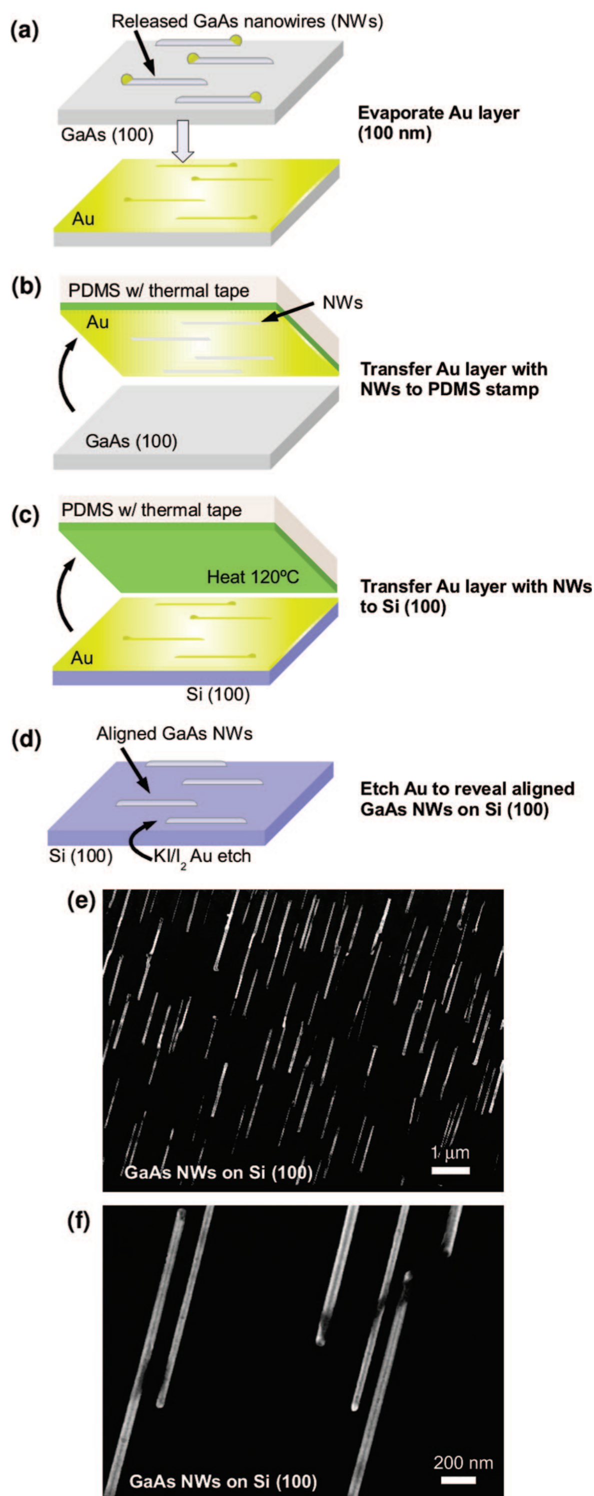

Figure 6. Schematic (a−d) of the process used to transfer highly aligned <110> GaAs nanowires to a Si (100) substrate: (a) GaAs nanowires are released from the growth substrate and covered with 100 nm of evaporated Au. (b) Au layer with nanowires is transferred to thermal release tape that is mounted onto a PDMS stamp. (c) PDMS/thermal tape and Au layer with nanowires is transferred to a Si (100) substrate and then heated to 120 °C allowing the thermal tape to release the Au layer onto the Si surface. (d) Au is wet etched with KI/I_2 to reveal aligned GaAs nanowires on Si surface. (e) Low-magnification SEM image of GaAs nanowires on Si surface. (f) High-magnification SEM image of GaAs nanowires on Si surface showing the precise alignment that is achievable with this transfer process.

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Supporting Information Available: This material is available free of charge via the Internet at http://pubs.acs.org.

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