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On-Chip Inductors with Self-Rolled-Up SiN_x Nanomembrane Tubes: A Novel Design Platform for Extreme Miniaturization

Wen Huang,[†,‡] Xin Yu,[†] Paul Froeter,[†] Ruimin Xu,[‡] Placid Ferreira,[§] and Xiuling Li*[,†]

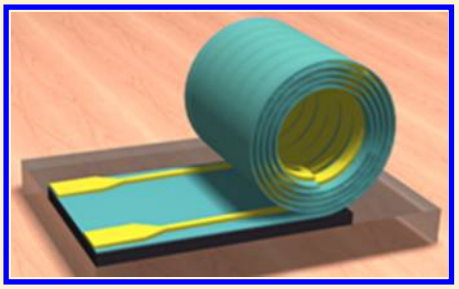
[†]Department of Electrical and Computer Engineering, Micro and Nanotechnology Laboratory, University of Illinois, Urbana, Illinois 61801, United States

[‡]EHF Key Laboratory of Fundamental Science, University of Electronic Science and Technology of China, Chengdu, Sichuan 611731, China

[§]Department of Mechanical Science and Engineering, University of Illinois, Urbana, Illinois 61801, United States

S *Supporting Information*

ABSTRACT: Inductors are essential components of radio frequency integrated circuits (RFICs). While the active devices in RF systems downscale steadily, inductors have not been able to keep up with the pace of continual miniaturization because of the trade-off between size and performance as well as fabrication complexity. Strain-induced self-rolled-up nanotechnology allows the formation of three-dimensional (3D) architectures, such as multiple-turn spiral tubes, through planar processing. Here, we report on using 3D SiN_x tubular structures with accompanying prepatterned metal layers, as a novel on-chip tube inductor design platform. We found, by an equivalent lumped circuit and electromagnetic modeling, that the 3D metal spiral structure has the ability to significantly better confine magnetic field compared to conventional planar spiral on-chip inductors. More than 100× reduction in footprint can be realized using this platform while achieving excellent electrical performance, including large inductance, high quality (Q) factor, and high self-resonance frequency (f_0).



KEYWORDS: *self-rolled-up, nanomembrane, on-chip inductor, SiN_x tube*

On-chip inductors have widespread applications in radio frequency integrated circuits (RFICs). Planar spiral inductor is the most commonly used on-chip inductor in current RFIC designs due to its easy fabrication with standard CMOS processes, which, at the same time, limits the design of on-chip inductors to be on a two-dimensional (2D) wafer surface.[1] Therefore, conventional planar spiral inductors have to utilize self-and mutual electromagnetic coupling of long parallel wires to achieve high inductance. A 10 nH, a planar spiral inductor usually takes up to ~400 × 400 μm^2 on-wafer area with typical maximum quality (Q) factor of ~6 at frequency lower than 3 GHz and self-resonance frequency of ~10 GHz.[2] The large footprint introduces significant parasitic coupling capacitance and ohmic loss from the substrate, which are the two main reasons for low Q factor and resonance frequency of planar spiral inductor.[3]

Efforts have been made for a long time to shrink the size and maintain or improve the performance of the on-chip planar spiral inductors. Among them, stacked planar spiral inductors were reported to occupy an area about 16% of that of conventional ones at a similar value of inductance.[4,5] Suspended MEMS spiral inductors with a Q factor as high as 20 at a frequency over 10 GHz were demonstrated.[6,7] Three dimensional (3D) microcoil inductors, with tunable inductance independent of their base dimensions, were shown to have a Q factor as high as 17 through metal deformation driven by thermal stress.[8] Intel corporation achieved high Q factors (>20) using planar inductors with footprint compatible with the 32 nm and beyond System on Chip (SoC) platform, but had to resort to a very thick low-resistivity top metal layer (4−7 μm).[9] All of these approaches only addressed some aspects of the outstanding issues with planar spiral inductors. This is because the 2D design limitation essentially leads to the trade-off of key characteristics of inductors, including on-wafer footprint, inductance, Q factor, resonance frequency, as well as fabrication cost and manufacturability.

Strain-induced self-rolled-up micro- and nanotubes are formed spontaneously when strained planar membranes deform driven by energy relaxation.[10−14] The strained membrane normally consists of an oppositely strained bilayer. Upon releasing from the substrate by etching away a sacrificial interlayer, the opposite force from each of the bilayers generates a net momentum, driving the planar membrane to scroll up and continue to roll into a tubular spiral structure. When putting metal strips on the strained bilayer, the metal thin film itself can also provide additional tensile residual stress to help the rolling.[15] Experimentally, thin films deposited by different methods or under different conditions have adjustable residual stresses in a wide range from 478 to −775.6 MPa for

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SiN_x and from >1000 MPa to < −1000 MPa for metal thin films on SiO_2.[16,17] By carefully designing the residual stress mismatch in each layer, it is possible to generate a large enough driving force to overcome resistance and continue rolling over a long enough distance to roll into as many turns as needed. As long as the thin membrane is strained and can be released from its mechanical support, self-rolled-up 3D architectures will form spontaneously with simply planar processing, as has been demonstrated for compound and elemental semiconductor material systems as well metal and dielectric materials including SiN_x.[18,19] The curvature of self-rolled-up tubes is determined by the thickness and inversely proportional to the net strain in the membrane. The typical wall thickness of a rolled-up dielectric tube is ∼10−100 nm, which yields a tube diameter of ∼1−10 μm. The number of turns can be controlled by predefining the size and shape of the membranes before rolling up. Diverse applications have been proposed theoretically and some have been demonstrated experimentally, including III−V quantum dot microtube lasers,[12] metamaterials based on arrays of gold/GaAs tubes,[20] optical tube resonators integrated with SOI waveguides,[21] and biological sensors using microtube resonators.[22] Recently, a metal (Ti/Cr)/insulator(Al_2O_3)/metal-(Ti/Cr) tube capacitor structure has been demonstrated experimentally for ultracompact energy storage. These tube capacitors are almost 2 orders of magnitude smaller than their planar counterparts.[23]

Here, we present an on-chip inductor design involving 3D multiple-turn metal spiral structures formed based on the self-rolled-up nanotechnology introduced above. As shown in Figure 1a, a square wave like patterned metal thin film layer was deposited on a strained SiN_x nanomembrane. By etching away the sacrificial layer, as shown in Figure 1b, metal strips will be rolled up together with the strained SiN_x nanomembrane to form 3D multiple-turn spirals. Each metal strip along the rolling direction, defined by its width w_s and length l_s, is called an inductor cell. All cells are connected in series by the connection lines, defined with its width w_c, and length l_c (the separation distance between cells). The patterned metal thin film layer is intended to be made as thick and smooth as possible to reduce the thin film resistivity but not too thick to stop the rolling process. Obviously, a standalone SiN_x nanomembrane inductor requires an even number of cells because its feedlines should be located on the same side. However, single-cell structure can be used together with other serially connected tube-based passive components. These rolled-up SiN_x nanomembrane inductors can further be transfer-printed and rearranged at will on wafers with predesigned RFICs.[24,25]

When AC current flows in and out the feedlines, time varying electromagnetic field will be triggered. Because the SiN_x thickness t_{SiN} (typically ∼40 nm) is very small compared to the tube radius R_1 (typically 0.5−5 μm), the radius change of each turn of the spiral structure is negligible. Therefore, the spiral structure can be treated electrically as multilayer closed concentric cylinders as illustrated in Figure 2a. R_1 is the inner radius, N_t is the number of turns, t_{SiNx} is the thickness of SiN_x membrane, and t_m is the thickness of metal thin film. Notice that the current flow directions in any adjacent cells are opposite, which introduces a cancellation mutual inductance M to each cell. Here we assume M is negligible when the coupling coefficient (M/L) of adjacent cells, where L is the self inductance, is less than 1%. However, the separation distance l_c needed to meet this requirement depends on the cell structure. For example, adjacent cells with more turns share

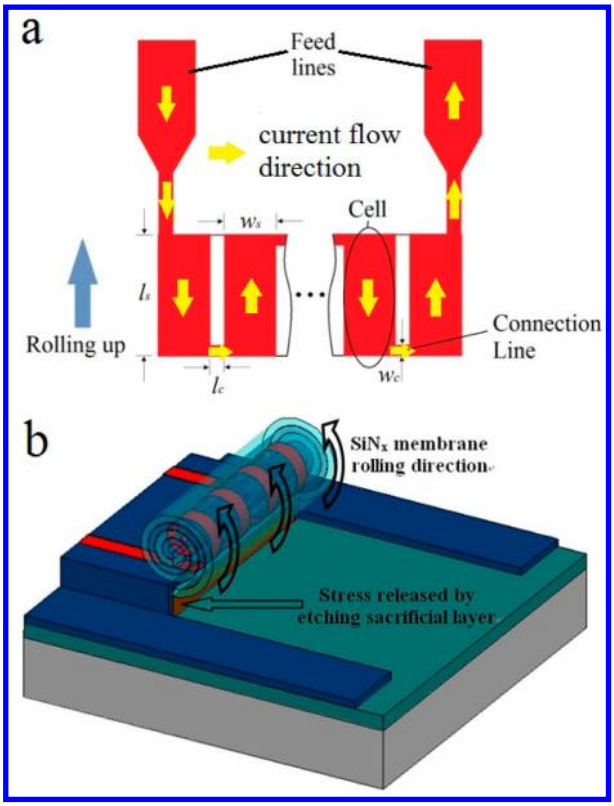

Figure 1. Schematic diagrams of the rolled-up SiN_x nanomembrane inductor structure, with structure parameters labeled. (a) Planar pattern of conduction strips before rolling up, with current flow direction indicated by the arrows. (b) Rolled-up conduction strips in a SiN_x multiturn nanomembrane spiral, with the membrane releasing mechanism and rolling direction indicated.

stronger magnetic flux density, therefore require larger l_c to reduce the mutual inductance M and vice versa. Notice that the shared magnetic flux density is inversely proportional to the cubic order of l_c (see Supporting Information eq S8), which means the coupling can be quickly reduced by separating adjacent cells further if there are more turns. Inevitable parasitic capacitances are produced by the coupling of conduction layers in the spiral, C_c, and by the substrate capacitance, C_s, respectively. When the conduction layers are made of metal, such as silver, copper, gold, or aluminum, the depth of penetration by skin effect at high frequency is much greater than the metal thickness.[2,26] This means that the RF mutual resistance between the metal thin film layers introduced by the eddy current effect is negligible and the ohmic loss is only caused by DC resistance R.[2] Also, the substrate loss induced by the substrate eddy current is not significant because of the small on-wafer footprint and the fact that the electromagnetic field is mostly confined in the cells not in the substrate (unlike the planar inductor). The lumped circuit model for two adjacent cells can then be built as shown in Figure 2c, and a number of (N) identical spiral cells connected in series is shown in Figure 2d (the magnetic coupling between any nonadjacent cells is ignored due to long separation distance). The parasitic connection line inductance L_c is negligible because we chose $l_s \gg l_c$. This lumped circuit model can be seen as a two-port π-type admittance network. The effective inductance L_{e_total}, Q factor Q_{total}, and self-resonance frequency f_0 can be then derived from the admittance matrix Y as follows:[2,27]

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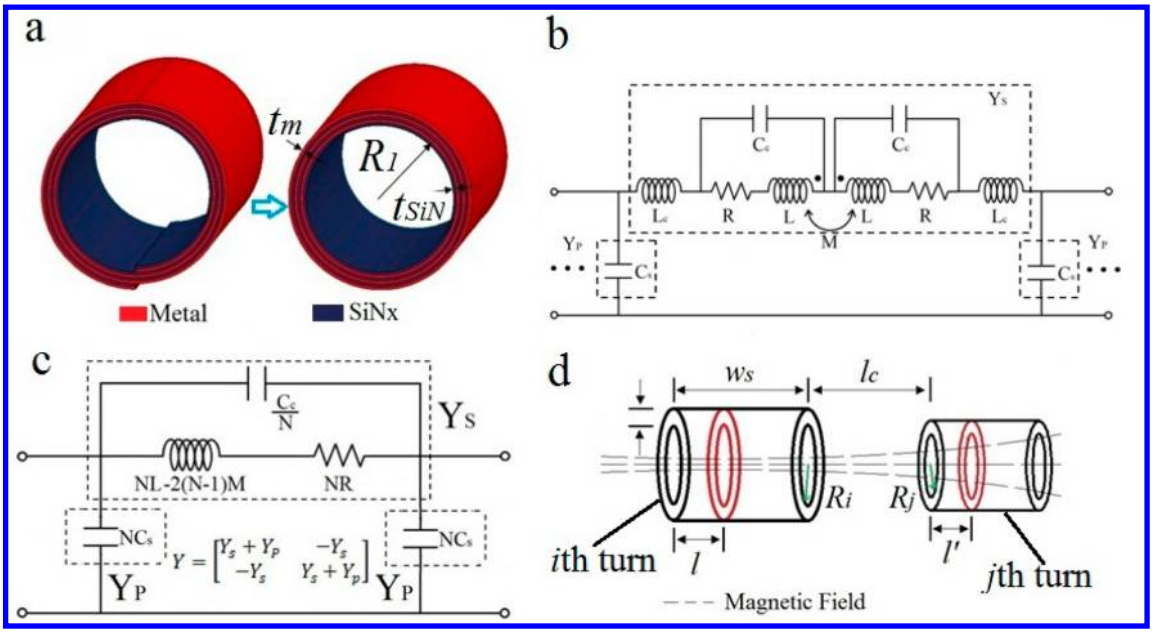

Figure 2. Lumped circuit physical model of rolled-up tube inductor. (a) Schematic showing the geometric definition using concentric cylinder assumption, (b) lumped circuit model for two adjacent cylindrical cells connected in series, (c) lumped circuit model for several (N) cylindrical cells connected in series, (d) magnetic coupling between any cylinder in adjacent cells.

$$L_{e\_total} = \frac{\mathrm{Im}\left(-\frac{1}{Y_{12}}\right)}{\omega} = \frac{\mathrm{Im}\left(\frac{1}{Y_s}\right)}{\omega} = \frac{N_c\{L' - C_c[R^2 + \omega^2(L')^2]\}}{1 + \omega^2 C_c^2[R^2 + \omega^2(L')^2] - 2\omega^2 C_c L'} \quad (1)$$

$$Q_{total} = \left|\frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})}\right| = \left|\frac{\mathrm{Im}(Y_p + Y_s)}{\mathrm{Re}(Y_p + Y_s)}\right| = \frac{\omega|L' - (C_c + N_c^2 C_s)[R^2 + \omega^2(L')^2]|}{R} \quad (2)$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{(C_c + N_c^2 C_s)L'} - \frac{R^2}{(L')^2}} \quad (3)$$

where $L' = L - 2((1 - N_c^{-1})M$, N_c is the number of cells, and L is the self-inductance of each cell (see Supporting Information for detailed derivations).

To simplify the calculation of M and L and obtain accurate expressions of them that can be embedded in a circuit level simulator, the magnetic flux density $\boldsymbol{B}(l)$ in each slice of a single layer cylinder (red slice in Figure 2d) is assumed to be uniform radially, but its value is dependent on the cylinder position and its inner radius. Then the mutual inductance M_{ij} between any two cylinders in adjacent cells (the ith cylinder in one cell and the jth cylinder in another cell as illustrated in Figure 2d) can be calculated by $M_{ij} = (\pi\mu_0 R_i^2)/(4t_m w_s^2)D_{ej}$, where $R_i = R_1 + (i - 1)\ t_{SiN}$, i = 1,2,3..., μ_0 is the permeability of air and D_{ej} denotes the geometric characteristic dimension (GCD) of the jth single-layer cylinder (see Supporting Information for detailed derivations). If l_c is set to be less than zero ($l_c < 0$) mathematically, it means that the two different turns Figure 2d physically overlap so that the beginning of the smaller turn is on the "negative" side of the end of the larger turn. When $l_c = -w_s$, the ith and jth single layer cylinders is equivalent to two different turns in one cell, and the self-inductance L_{self} of the ith single layer cylinder and mutual inductance L_{mutual} between the ith and jth single layer cylinders in one cell can be expressed as $L_{self\_tt} = M_{ij}|_{i=j,l_c=-w_s}$, $L_{mutual\_ij} = M_{ij|i\neq j,l_c=-w_s}$, respectively. The total inductance L of multilayer concentric cylinders can then be expressed by the sum of all L_{self_ii} and L_{mutual_ij}, i = 1,2,3...N_t, j = 1,2,3...N_t, and the mutual inductance M can then be expressed by the sum of all M_{ij}, i = 1,2,3...N_t, j = 1,2,3...N_t with $l_c > 0$.

Because the distance between the metal layers of each turn is very small ($\Delta R \sim 40$ nm), the adjacent metal layers are not equipotential under high frequency operation and therefore the crosstalk capacitance cannot be neglected.[1,17] We use the sum of all overlap capacitances in the equivalent structure to represent the crosstalk distribution capacitance $C_c = (2\pi\varepsilon_{SiN}w_s)/(\ln[1 + (t_{SiN}(N_t - 1))/(R_1)])$, which can be approximated, similar to that of coaxial capacitor. Substrate parasitic capacitance C_s of one cell is approximately proportional to the projection area on the substrate by the metal spirals and connection lines. C_s can be estimated by $1/2\{2w_s[R_1 + N_t t_m + (N_t - 1)t_{SiN}] + w_c l_c\}C_{sub}$. The factor two in the denominator accounts for the fact that the substrate parasitic capacitance is assumed to be distributed equally at the two ends of the inductor. C_{sub} is the capacitance per unit area of the silicon substrate, which is a function of the substrate doping. In our calculation and simulation, the resistivity of the silicon substrate is assumed to be 10 Ω·cm and the corresponding C_{sub} is 1.6×10^{-3} fF/μm^2.[2] As discussed before, the resistance of a cell is calculated by DC resistance formula $R \approx \rho l_s/w_s t$ without eddy current effect, where ρ is the resistivity of the metal thin film. However, the resistivity value of a certain metal thin film depends on several fabrication and environment factors, including the thickness, the mean square root surface

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roughness, and the operating temperature when current passes through it. We first used the resistivity values of bulk metal material, including silver (1.59 $\mu\Omega$·cm), copper (1.72 $\mu\Omega$·cm), gold (2.44 $\mu\Omega$·cm), and aluminum (2.82 $\mu\Omega$·cm), to give the best theoretical performance of the tube inductor. The effect of metal thin film properties and structural characteristics on the inductor electrical performance, especially the Q factor, was then analyzed.

The lumped circuit physical model developed above allows us to evaluate a comprehensive set of tube structural parameters on the inductor performance quickly. The accuracy of the model was confirmed using the commercial software high frequency structure simulator (HFSS) (see Supporting Information). Shown in parts a and b of Figure 3 are the

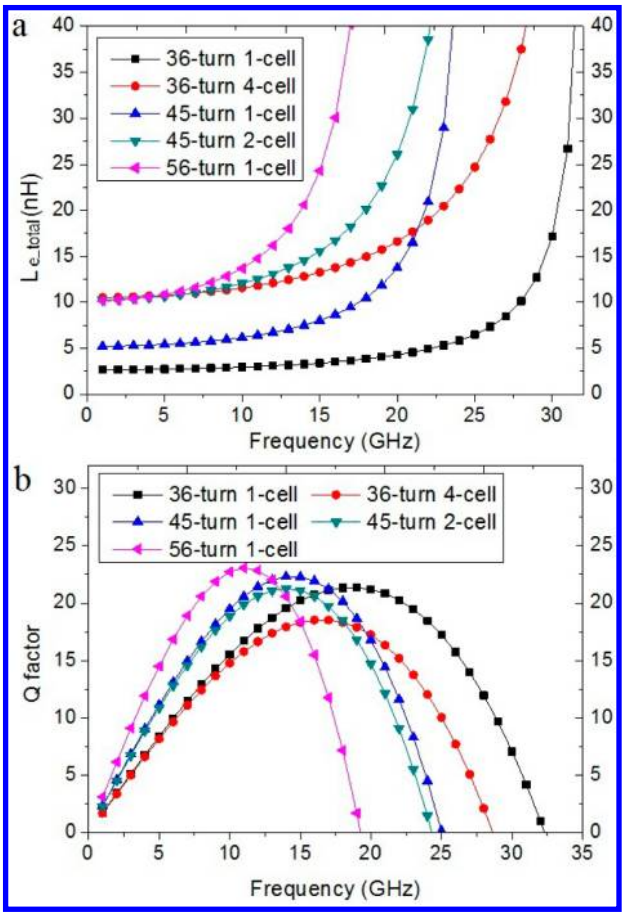

Figure 3. Self-rolled-up SiN_x nanomembrane inductor performance as a function of number of turns and number of connected cells. (a) Effective inductance L_{e_total} vs operating frequency. (b) Corresponding Q factor vs operating frequency. The metal strip is assumed to be 100 nm thick, 15 μm wide Ag. The inner diameter of the rolled-up tube is assumed to be 3 μm (with 40 nm thick SiN_x), and the separation distance between each cell is 15 μm.

effect of number of turns (rotations in the self-rolled-up tube) and number of lateral unit cells on the total effective inductance L_{e_total} and Q factor as a function of operating frequency. It can be seen that large inductance values L_{e_total} can be obtained by increasing the number of turns in each cell or connecting more cells in series. The designs with fewer cells have better Q factor and smaller footprint but lower self-resonance frequency due to larger parasitic capacitance C_c from serially connected cells in the spiral.

In contrast to planar spiral inductors, the Q factor and self-resonance frequency still remain high when connecting more cells in the self-rolled-up 3D spiral structures because of their weak dependence on the number of cells N_c due to extremely small substrate capacitance C_s (implied from eqs 2 and 3). Extreme reduction of footprint can be realized while maintaining or enhancing the performance. For example, a design consisting of a 45-turn 2-cell tube inductor with 3 μm inner diameter, 15 μm cell separation distance, 40 nm thick SiN_x membrane, 15 μm wide, and 100 nm thick silver line will have a total effective inductance of 10 nH, maximum Q factor of 21 at 15 GHz, self-resonance frequency at 25 GHz, and 45 × 16 μm^2 occupied wafer area, This footprint is 0.45% of that of a conventional planar spiral inductor (typical values: 400 × 400 μm^2, 8 nH inductance, maximum Q factor is 6 at 3 GHz).[28] For single cell design, 56-turn inductor with otherwise the same structure parameters as the 2-cell design above is required to reach 10 nH. Remarkably, this design has a maximum Q factor of over 23 at 11 GHz and occupies only 15 × 19 μm^2 wafer area, which is about 0.1% of that of conventional planar spiral inductors.

For a nanomembrane inductor with a certain number of cells and turns, the dimension and fabrication quality of the dielectric (e.g. SiN_x) membrane and metal thin film can affect the inductor's performance. It was reported that a deposition thickness as large as 300 nm was needed to reach acceptable sheet resistivity (~2 $\mu\Omega$·cm) for Ag thin film,[29] which will lead to large rolled-up tube diameter and may even stop the self-rolling process. On the other hand, low resistivity Ag–W thin film was reported to exhibit a sheet resistivity ~4 $\mu\Omega$·cm with ~100 nm thickness,[30−32] which is an acceptable thickness for rolling experimentally. Parts a and b of Figure 4 show the calculated Q factor and total effective inductance L_{e_total}, respectively, for various sheet resistivity values. Clearly, high resistivity directly leads to reduction of the Q factor, while it does not change the inductance much until the frequency reaches about 25 GHz. Because the Q factor is determined by the total DC sheet resistance R of metal thin film strips, when the metal thickness and sheet resistivity are fixed, the value of R can be reduced by increasing the width w_s of strip. However, as shown in Figure 4c, the wider the width w_s is, the smaller the total effective inductance L_{e_total} becomes. The reduction of L_{e_total} indicates weaker magnetic energy storage ability, which consequently results in only a small increase of Q factor as shown in Figure 4d. In addition, although inductance is mainly affected by the inductor size and structure, large resistivity of the metal thin film can also have a noticeable negative impact on it due to significant ohmic loss. For example, when the resistivity of the metal thin film is 30 $\mu\Omega$·cm instead of 4 $\mu\Omega$·cm for the same device in Figure 4a, the maximum Q factor will be lower than 1 and the inductance will drop by 10%. All of the above analysis underlines the importance of optimizing the thin film metal resistivity to realize the full potential of the rolled-up tube inductor platform.

In conclusion, we have presented a novel design platform for on-chip inductors based on strain-induced self-rolled-up nanotechnology, which produces 3D architectures through simply planar processing. Its 3D spiral architecture contributes directly to better confining the magnetic field and therefore enhancing the magnetic energy storage ability to obtain high inductance with dramatically smaller footprint and reduced substrate parasitic capacitance. Preliminary experimental data on prototype tube inductor with a few turns show measured

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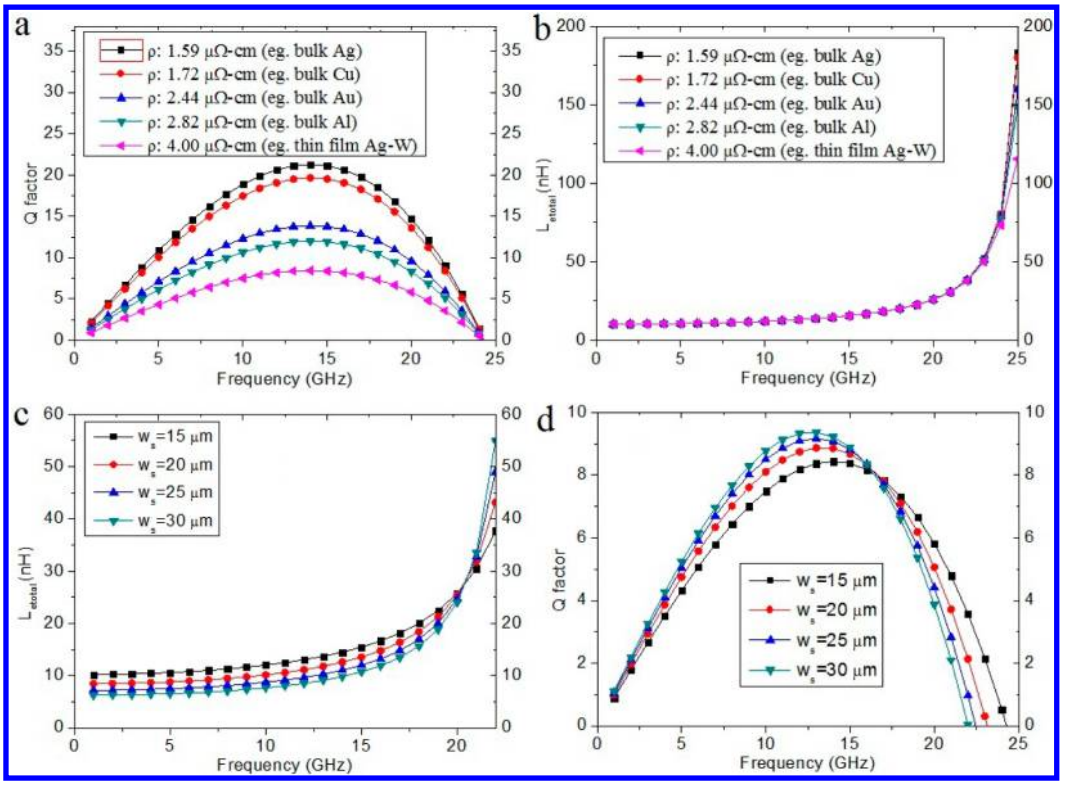

Figure 4. SiN_x nanomembrane inductor performances, Q factor Q_{total} (a,d), and total effective inductance $L_{e\_total,}$ (c,d) as a function of metal sheet resistivity ρ (a,b) and metal strip width w_s (c,d) for a 45-turn 2-cell inductor operating in a frequency range of 1−25 GHz. The tube inner diameter is set to be 3 μm, and the separation distance between the two cells is 15 μm. The metal strip thickness is 100 nm for all cases. The metal strip widths for (a) and (b) are 15 μm, and the sheet resistivity for (c) and (d) is 4.0 $\mu\Omega$·cm (Ag−W thin film).

inductance consistent with designed values, and experimental development toward the ideal structures is underway and will be reported separately. In addition to inductors, rolled-up tube-based capacitors and resistors can also be fabricated by this technology and integrated together with the rolled-up tube inductors for a super miniaturized passive RFIC platform.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Derivation of effective inductance, Q factor, and self-resonance frequency of tube inductors. Derivation of self inductance, mutual inductance, and parasitic capacitances of 3D multiturn spiral structures. Verification of the developed lumped circuit physical model by HFSS simulation. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author

*Phone: +1 (217)265-6354. Fax: +1(217)244-6375. E-mail: xiuling@illinois.edu.

Author Contributions

The idea in this manuscript was first proposed by Xiuling Li and Placid Ferreira. Modeling and simulation were performed by Wen Huang and Xin Yu. Discussions and analysis were done by all authors and the manuscript was mainly written by Wen Huang, Xiuling Li, and Xin Yu. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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