

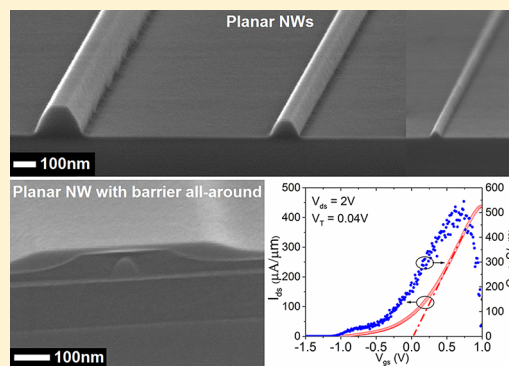
Monolithic Barrier-All-Around High Electron Mobility Transistor with Planar GaAs Nanowire Channel

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ABSTRACT: High-quality growth of planar GaAs nanowires (NWs) with widths as small as 35 nm is realized by comprehensively mapping the parameter space of group III flow, V/III ratio, and temperature as the size of the NWs scales down. Using a growth mode modulation scheme for the NW and thin film barrier layers, monolithically integrated AlGaAs barrier-all-around planar GaAs NW high electron mobility transistors (NW-HEMTs) are achieved. The peak extrinsic transconductance, drive current, and effective electron velocity are $550 \mu\text{S}/\mu\text{m}$, $435 \mu\text{A}/\mu\text{m}$, and $\sim 2.9 \times 10^7 \text{ cm/s}$, respectively, at 2 V supply voltage with a gate length of 120 nm. The excellent DC performance demonstrated here shows the potential of this bottom-up planar NW technology for low-power high-speed very-large-scale-integration (VLSI) circuits.

KEYWORDS: GaAs, nanowire, high-electron-mobility transistors, III–V, VLSI



Owing to their self-assembled small feature size and inherent 3D cross-section, semiconductor NWs grown through bottom-up methods have been studied heavily for the past decade for their potential use in future low power and high speed electronics.^{1,2} NW MESFETs,^{3–5} MOSFETs,^{6–8} HEMTs,^{9–12} and NW CMOS inverters and ring oscillators¹³ made from self-assembled vertical NWs have been demonstrated. However, to make NW based very large scale integrated circuits (VLSI), major challenges including controllability of NW position, uniformity of NW electrical property,^{14–16} and compatibility with planar processing remain to be fully addressed.

Recently, we have developed a method of growing planar GaAs NWs on both (100) and (110) GaAs substrates using metal organic chemical vapor deposition (MOCVD) through gold (Au) catalyzed vapor–liquid–solid (VLS) mechanism.^{5,17–19} In contrast to conventional out-of-plane $\langle 111 \rangle$ NWs, these planar NWs grow self-aligned and epitaxially on the substrate surface. Unlike vertical NW-FETs and postgrowth externally aligned planar NW-FETs, self-assembled planar NW-FET geometry is fully compatible with planar processing. The positions of the planar NW-FETs can also be precisely determined through patterning the Au catalysts. Planar GaAs NWs have been proven to have the same electron transport properties as defect-free bulk GaAs by the study of planar GaAs MESFETs.^{4,5} We have also fabricated multiple channel planar GaAs NW-HEMTs with self-aligned intrinsic planar $\langle 110 \rangle$ GaAs NWs capped with Si doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ thin film as the channel on semi-insulating (100) GaAs substrates and demonstrated the feasibility of wafer-scale electrical uniformity of bottom-up NW-FETs.¹² These prototype devices are of 1.2 μm gate length with NWs of $\sim 250 \text{ nm}$ diameter as the channel.

To improve planar NW-HEMT performance, it is imperative to scale both the size of NWs and the gate length. As is well-known, the diameters of VLS NWs are determined by the size of Au catalysts. However, down-scaling planar NWs simply by using Au catalysts of smaller size were not successful due to more severe parasitic NW sidewall deposition during VLS growth. In this Letter, we report a method of growing high quality sub-50 nm planar GaAs NWs developed by mapping the growth parameter space out of the conventional boundary, and the first NW-HEMT with monolithically integrated barrier-all-around planar GaAs NW as the channel.

The growth of planar GaAs NWs was carried out on semi-insulating GaAs (100) substrates in an Aixtron 200 MOCVD reactor under atmospheric pressure. As reported previously, planar GaAs NWs propagate in the $[0-11]$ or $[01-1]$ directions.¹⁷ The standard growth condition for these planar NWs is at 460 °C with 5 sccm ($5.78 \times 10^{-5} \text{ mol/min}$) trimethylgallium (TMGa), and a nominal group V (AsH_3) to group III (TMGa) molar ratio (V/III ratio) of 32. Since planar $\langle 110 \rangle$ GaAs NWs have an isosceles-trapezoidal radial cross-section with $\langle 111 \rangle$ sidewall facets, a $\langle 100 \rangle$ top facet, and a base angle of 54.7° , top and cross-section view of planar NWs is used to illustrate the quality of the NW morphology. Shown in Figure 1a–c are top and cross-section view SEM images of as-grown GaAs NWs catalyzed using Au nanoparticles of 250 nm, 100 nm, and 20 nm diameters on the same substrate in the same growth run under the standard growth condition mentioned above. Compared with NWs seeded by 250 nm

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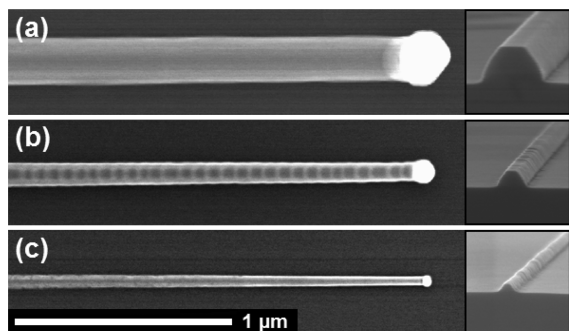


Figure 1. Top and cross-section view SEM images of as-grown GaAs NWs catalyzed using (a) 250 nm, (b) 100 nm, and (c) 20 nm diameter Au nanoparticles on the same substrate in the same growth run under the standard growth condition: atmosphere pressure, growth temperature of 460 °C, 5 sccm TMGa flow, and V/III ratio of 32. All images share the same scale bar.

Au catalysts, NWs seeded by 100 nm and 20 nm Au catalysts have rougher sidewall facets, more tapering along the axial direction, and noticeable notches perpendicular to axial direction throughout the full length of the NWs. As have been observed by TEM and also reported in binary III–V vertical NW systems,^{20–22} the notches are correlated with twin plane defects, suggesting that 250 nm Au catalysts seeded NWs are nearly twin-defect-free, while NWs seeded by smaller Au catalysts have lots of twin defects. Surface roughness, tapering, and twin defects could all be detrimental for NW devices aiming for high mobility and uniform electrical properties. Therefore, down-scaling of the NW size is not straightforward, and the growth condition must be retuned to realize high-performance down-scaled planar NW devices.

While keeping the same growth temperature (460 °C), pressure (atmospheric), and V/III ratio (32) as in the standard growth recipe, we varied TMGa flow from 2.5 to 10 sccm in steps of 2.5 sccm to study the effect of group III flow on planar NW growth. In each of the growth, we loaded two samples with 100 nm and 20 nm Au catalysts, respectively. The growth time (t_g) was kept constant at 140 s for all samples. After growth, each sample was inspected in SEM to measure the average length of NWs and bottom cross-section widths at the beginning (W_b) and end (W_e) of the NWs. $[(W_b - W_e) \sin(54.7^\circ)]/2t_g$ gives the radial growth rate (R_{radial}) of parasitic film, while the axial growth rate (R_{axial}) of planar NWs is simply the length of NWs divided by the growth time. Figure 2 plots the axial and radial growth rates of 100 nm and 20 nm Au catalysts seeded planar NWs under various group III flows. Clearly, as the group III flow increases, R_{axial} increases monotonically while R_{radial} stays relatively the same. Therefore, planar NWs grown under large group III flows not only grow faster but also become less tapered. In fact, by changing the group III flow from 2.5 to 10 sccm, the tapering factor, that is the deposition of parasitic film in radial direction per μm increment of NW in axial direction, is reduced from 7.9 to 2.4 $\text{nm}/\mu\text{m}$ and 8.4 to 1.5 $\text{nm}/\mu\text{m}$ for 100 nm and 20 nm Au seeded NWs, respectively.

We then kept the TMGa flow at 10 sccm and adjusted only the AsH_3 flow to check the effect of V/III ratio on planar NW growth. Growth experiments were done under V/III of 32, 16, 8, and 4, respectively. The same measurement of R_{axial} and R_{radial} was carried for samples under each growth condition. Figure 3 plots the axial and radial growth rates of 100 nm and 20 nm Au

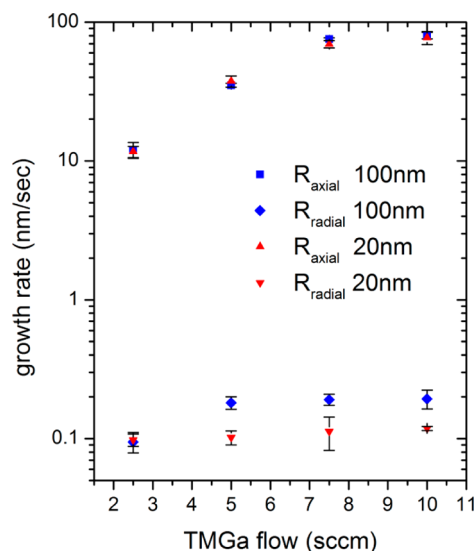


Figure 2. Axial (upper symbols) and radial (lower symbols) growth rates of 100 nm (blue squares) and 20 nm (red triangles) Au seeded planar NWs under group III flows of 2.5, 5, 7.5, and 10 sccm. All samples were grown at 460 °C and under the same V/III ratio of 32. The vertical bars on the symbols represent the range of data points collected from different NWs.

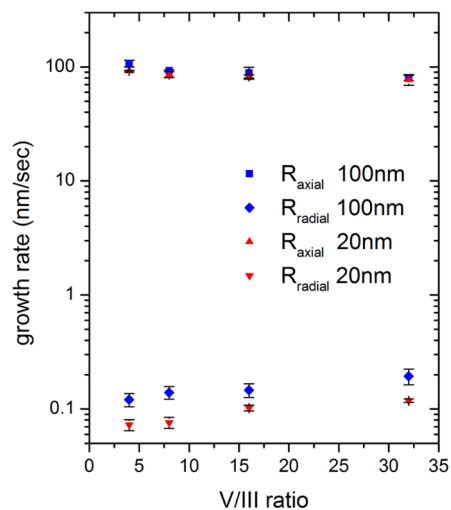


Figure 3. Axial (upper symbols) and radial (lower symbols) growth rates of 100 nm (blue squares) and 20 nm (red triangles) Au catalysts seeded planar NWs under V/III ratios of 4, 8, 16, and 32. All samples were grown at 460 °C and under the same group III flow of 10 sccm.

catalysts seeded planar NWs under various V/III ratios. Different from vertical GaAs NW growth, for which both R_{axial} and R_{radial} decrease as the V/III ratio decreases,²³ the R_{axial} increases, while R_{radial} decreases for planar NW growth. Thus, by changing the V/III ratio from 32 to 4, the tapering factor is further reduced from 2.4 to 1.1 $\text{nm}/\mu\text{m}$ and 1.5 to 0.8 $\text{nm}/\mu\text{m}$ for 100 nm and 20 nm Au catalysts seeded NWs, respectively. However, we still noticed twin-plane defects induced notches under such growth conditions.

To grow twin-defect-free down-scaled planar NWs, we have investigated the temperature effect on planar NW growth. The pyrolysis efficiency of TMGa quickly drops when the growth temperature is below 450 °C. Thus growing planar NWs below 450 °C would further suppress the parasitic film growth.

Because the Au–Ga alloy selectively assists the decomposition of TMGa, the effective Ga supply for axial NW growth should not be affected much and may even increase due to the suppressed Ga incorporation in parasitic film. However, the yield of planar NWs (vs out-of-plane NWs) is sensitive to growth temperature. If we start growing NWs below 460 °C, the yield of planar NWs will be low. To maintain high yield of planar NWs but grow planar NWs under low temperature, we have adopted a two-temperature-step growth method.²⁴ We start the planar NW growth at 460 °C for a brief time period (20 s) and then quickly drop the temperature to a lower temperature (T_{target}). As long as the planar NWs growth mode is initiated in the brief 460 °C growth period, planar NWs keep growing planar at the lower temperature T_{target} .¹⁷ If dropping the temperature too low, planar NWs will finally take off in $\langle 111 \rangle$ B directions; this defines the lower bound of T_{target} . Under growth condition of atmosphere pressure and TMGa flow of 10 sccm, the lower bound of T_{target} is 425 °C and independent of how the temperature is dropped (quick or slow). In a set of controlled experiments, we set T_{target} to 435 °C, the total NW growth time to 140 s, TMGa flow to 10 sccm and varied the V/III ratio. With the combined effects of low V/III ratio and low growth temperature, we have achieved defect-free high quality planar NWs with sub-50 nm diameter as shown in Figure 4a–b. Figure 4a shows the cross-section view

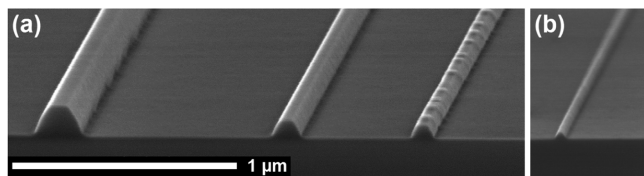


Figure 4. (a) Tilted cross-section view of planar GaAs NWs seeded by Au catalysts with 250, 150, and 100 nm diameters (from left to right) using the two-temperature-step (460 → 435 °C) and V/III ratio of 6 growth method with 10 sccm TMGa flow; the notches induced by twin-plane defects in the 100 nm Au seeded NW are clearly visible. (b) Notch-free sub-50 nm planar GaAs NW seeded by Au catalyst with 20 nm diameter with the change of V/III ratio from 6 to 4. All images share the same scale bar.

of three planar NWs seeded by 250 nm, 150 nm, and 100 nm Au particles under V/III ratio of 6. The size-dependence of defect density in planar NWs is clear: while 250 nm and 150 nm Au catalysts seeded NWs have no twin defects induced notches under such growth condition, the 100 nm Au particle seeded NWs still have many. When dropping the V/III ratio to 4, the twin defects induced notches can be completely eliminated for all planar NWs seeded by Au catalysts with diameters larger than 20 nm. Figure 4b shows the cross-section view of a defect-free planar NW seeded by 20 nm Au particle under a V/III ratio of 4. Measurement of the growth rate also confirmed that, although growing under lower temperature, the R_{axial} in two-temperature-step growth is slightly higher than in single temperature growth at 460 °C. In summary, by using a two-temperature-step (460 → 435 °C) growth method with 10 sccm TMGa flow and V/III ratio of 4, we have for the first time achieved defect-free high quality sub-50 nm GaAs NWs.

With the capability of growing defect-free high quality sub-50 nm planar NWs, we continue to optimize the growth of NW-HEMT structure. The normal procedure of NW-HEMT growth starts with planar GaAs NW VLS growth and proceeds to epitaxial thin film growth by lowering the reactor pressure to

100 mbar and raising the growth temperature to 680 °C. The epitaxial thin film composes 3 nm undoped $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ as the spacer layer, Si-doped ($2 \times 10^{18} \text{ cm}^{-3}$) $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ as the top barrier, and n^+ GaAs as the source and drain ohmic contact layer. However, small planar NWs are thermally vulnerable to high temperature processes. While elevating the growth temperature up to 680 °C with as-grown planar GaAs NWs, they deform into flat shapes before being coated by $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ and GaAs thin film even under AsH_3 overpressure, as shown in the top inset of Figure 5 where diluted

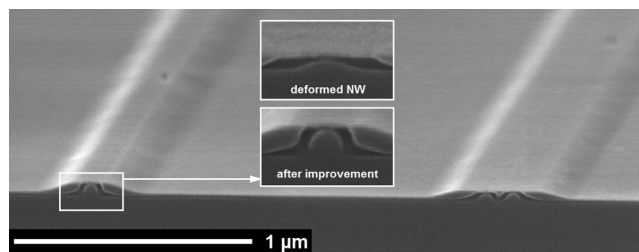


Figure 5. Tilted cross-section view of NW-HEMTs with high quality 20 nm Au catalysts seeded single and double NW channels. Diluted HF was used to selectively etch off $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ and reveal contrast between $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ and GaAs. Insets illustrate the comparison between NW-HEMTs with deformed and high quality 20 nm Au catalyst seeded NW as channels.

HF was used to selectively etch off $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ and reveal contrast between $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ thin film and the GaAs NW. The deformed planar NWs have a lower aspect ratio and weakens its advantage in 3D electrostatic control. Trial experiments with epitaxial top layers grown at 600 °C still rendered deformed planar NWs. We then employed a two-temperature-step method on growing the top epitaxial layers: coat and protect planar NWs with 3 nm undoped $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ at 500 °C, then grow successive layers at 680 °C. Because the undoped $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ is much more stable than GaAs, with its protection, the planar NWs can maintain their original morphology during the subsequent high temperature processes (Figure 5). The right side image in Figure 5 shows two side-by-side planar GaAs NWs with less than 20 nm separation and common top epitaxial layers. This high level of 3D channel integration can hardly be achieved by top-down processes through lithography.

Finally, we fabricated short-channel barrier-all-around planar NW-HEMTs to explore planar NWs' potentials for future low power high speed device applications. Prior to the growth of planar NWs and top epitaxial layers, we grew an intrinsic 150 nm thick $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ back barrier at 680 °C in order to improve carrier confinement. Previously dispersed 100 nm Au catalysts under such growth conditions simply elevated to the top surface, and no NW growth took place.¹⁷ Then 15 μm long planar NWs were grown and covered with 3 nm undoped $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ spacer, thick Si-doped ($2 \times 10^{18} \text{ cm}^{-3}$) $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ top barrier, and n^+ GaAs ohmic contact layer. The tilted cross-section SEM image of as-grown NW-HEMT is shown in Figure 6a where $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ top and back barriers were selectively etched off by diluted HF. The process flow of fabricating planar NW-HEMTs is similar to conventional thin film HEMTs: source and drain formation was done first followed by mesa isolation, gate recess etch, and gate metal evaporation. Since we were using randomly dispersed 100 nm Au catalysts as planar NW growth seeds for this study, we

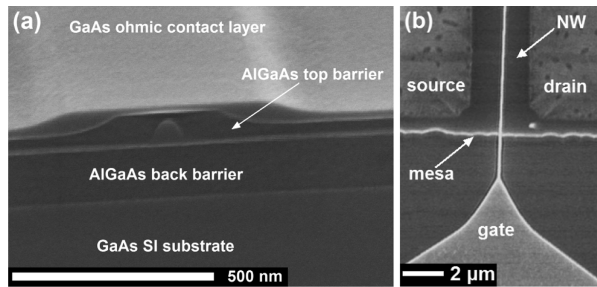


Figure 6. (a) Tilted cross-section view of NW-HEMT with barrier-all-around planar GaAs NW as the channel. $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ was selectively etched by dilute HF to reveal contrast. (b) Top view of a fully-fabricated short-channel NW-HEMT with a 120 nm gate, 3 μm source to drain separation, and single barrier-all-around planar NW channel as shown in part a (the other mesa edge is $\sim 20 \mu\text{m}$ away and not shown here).

intentionally made the source and drain metal pads to be 20 μm wide to increase the chance of having planar NWs in between. Figure 6b is the top-view SEM image of a fully-fabricated short-channel NW-HEMT with a 120 nm gate, 3 μm source to drain separation, and single barrier-all-around planar NW channel as indicated in Figure 6a. Figure 7a shows the output characteristics of this specific device with gate bias ranges from -0.9 to 0.5 V in steps of 0.2 V. Figure 7b plots the transfer characteristics at 2 V drain bias scaled by $W = 145$ nm, where W is the periphery of all conducting surfaces: the single planar NW channel's two side walls and top facet. The peak extrinsic transconductance ($G_{m\text{-ext}}$) is $550 \mu\text{S}/\mu\text{m}$ and peak drive current ($I_{d\text{-max}}$) is $435 \mu\text{A}/\mu\text{m}$. $I_{\text{on}}/I_{\text{off}}$ ratio of 10^4 , subthreshold slope of 160 mV/dec and DIBL of 120 mV/V are extracted from family of transfer curves in log scale (Figure 7c).

Table 1 benchmarks the performance of our NW-HEMTs against the state-of-art III–V FETs in other geometries, including the quantum well (QW) based InAlAs/InGaAs HEMTs,¹ top-down etched InGaAs, and vertically grown InAs NW gate-all-around (GAA) MOSFETs.^{2,8} Note that the AlGaAs top barrier in our NW-HEMT (Figure 6a) is much thicker than that in the QW HEMTs.¹ This leads to small gate capacitance and large source/drain access resistance, which must be compensated by high effective electron velocity (ν_{eff}) to support comparable device performance. ν_{eff} of $\sim 2.9 \times 10^7$, 2.6×10^7 , and 1.7×10^7 cm/s have been extracted for our NW-HEMT at $V_{\text{ds}} = 2$, 1, and 0.5 V, respectively. For comparison, the ν_{eff} of all other devices in Table 1 are also estimated the same way, as explained in the footnote of Table 1. Although having the largest L_{g} , our NW-HEMT shows very high ν_{eff} and thus high degree of velocity overshoot,²⁵ indicating excellent channel material property: large mean free path and high low-field electron mobility.²⁶ As for the non-ideal $I_{d\text{-max}}$, $G_{m\text{-ext}}$ and SS, we believe they can be improved by applying delta doping in a uniform and thin AlGaAs top barrier, which should enhance gate electrostatic control while reducing the source/drain access resistance. In addition, by customizing the mesa width to the width of NW-HEMT's channel, the gate and junction leakage through the non-channel regions, which is currently defined by the $\sim 20 \mu\text{m}$ wide mesa, should be greatly suppressed.

In summary, we have reported a method of growing down-scaled planar GaAs NWs with sub-50 nm width under conditions of high group III flow, low V/III ratio, and $460 \rightarrow 435$ °C two-step growth. This method has produced smooth

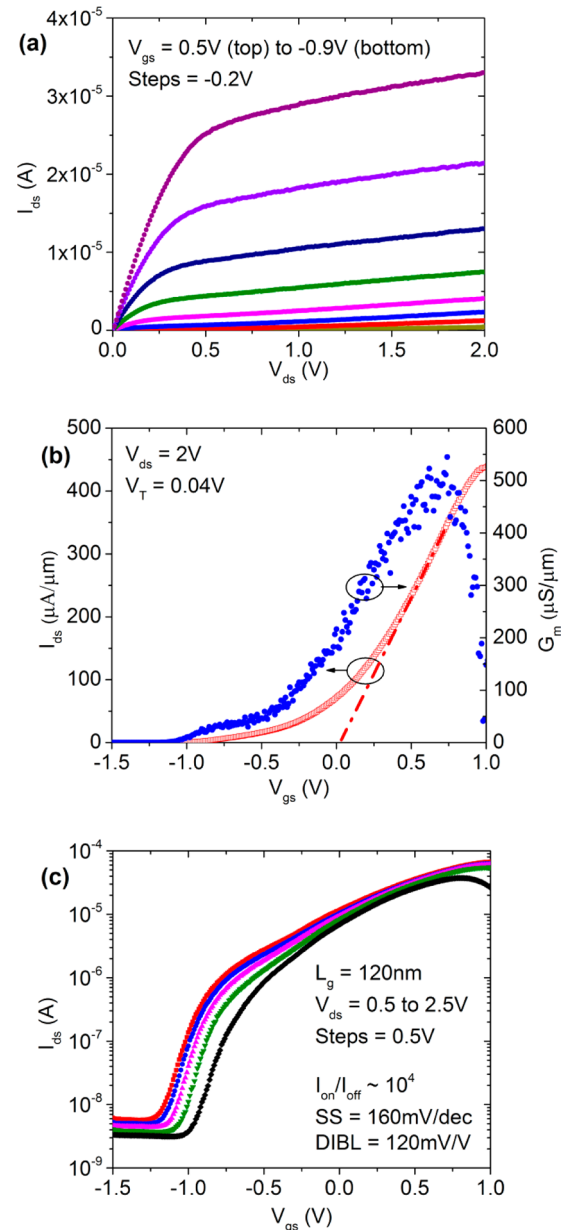


Figure 7. DC characteristics of the NW-HEMT shown in Figure 6. (a) Output characteristics with gate bias ranges from -0.9 to 0.5 V in steps of 0.2 V. (b) Transfer characteristics at $V_{\text{ds}} = 2$ V scaled by $W = 145$ nm (periphery of the single planar NW channel's two side walls and top facet). (c) Family of transfer curves in log scale.

planar NWs with extremely uniform cross sections, with a tapering factor of better than 1:1000. We have also demonstrated the growth of NW-HEMTs structures with monolithically integrated barrier-all-around planar GaAs NW channels. A short-channel single planar GaAs NW-HEMT, grown under the optimized growth condition monolithically, demonstrated excellent device performance. With further development of our planar NW technology as well as device layout improvement as discussed, wafer-scale low power and high speed VLSI circuits involving narrow planar NWs with 3D cross sections grown from the bottom-up is promising.

Table 1. Benchmarking the Device Performance of Our NW-HEMTs against the State-of-Art III–V FETs in Other Geometries

ref.	geometry	L_g (nm)	V_{dd} (V)	I_{d-max} (A/mm)	G_{m-ext} (S/mm)	SS (mV/dec)	estimated ^a v_{eff} ($\times 10^7$ cm/s)
this work	GaAs NW-HEMT	120	1.0	0.38	0.50	160	2.6
1	In _{0.7} Ga _{0.3} As QW-HEMT	40	0.6	0.96	2.70	115	3.0
2	In _{0.53} Ga _{0.47} As GAA-MOS	20	0.5	0.63	1.74	88	1.2
8	InAs GAA-MOS	100	0.5	0.60	1.23	140	0.6

^a v_{eff} is the average electron velocity under gate and calculated using the relationship G_{m-int}/C_{ox}^{26} . G_{m-int} was estimated through $G_{m-ext}/(1 - R_s G_{m-ext})$, where R_s is the source access resistance. C_{ox} was estimated through $\epsilon/(d + \Delta d)$, where ϵ is the gate dielectric permittivity, d is the effective distance between gate to channel, and Δd is the effective distance between the peak of the electron wave function and the physical interface. To estimate G_{m-int} , we assigned 25% of the on resistance ($R_{ON} \sim 1.82 \Omega\text{-mm}$) to R_s (considering the thick AlGaAs barrier). To estimate C_{ox} , the effective electrostatic thickness $d = 38$ nm was extracted by averaging the total effective gate capacitance from the NW sidewalls (capacitors with inclined plates) and NW top facet (capacitor with parallel plates); and 8 nm was assumed for Δd .²⁷ The essential parameters used for v_{eff} estimation of other devices in the table have been extracted from the referenced work.

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Notes

The authors declare no competing financial interest.

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