Scalable Monolithically Grown AlGaAs–GaAs Planar Nanowire High-Electron-Mobility Transistor

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***Abstract*—Monolithically grown planar nanowire (NW) high-electron-mobility transistors (NW-HEMTs) are demonstrated using self-aligned $\langle 110 \rangle$ GaAs NWs capped with Si-doped $Al_xGa_{1-x}As$ shell as the channel on semi-insulating (100) GaAs substrates. The planar $Al_{0.35}Ga_{0.65}As$–GaAs NW-HEMT with $\sim$ 1-μm-long gate exhibits excellent dc characteristics, with extrinsic G_m of $\sim$80 mS/mm and estimated intrinsic G_m of $\sim$260 mS/mm, where the device width is defined as the entire periphery of the NWs. The $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio is $\sim 10^4$ and the threshold is -1.5 V operating in depletion mode. The output current increases linearly with the number of NWs in the channel, while the threshold voltage does not change at all. This indicates excellent uniformity and scalability of the bottom-up-grown NW devices. Compared to field-effect transistors with doped NWs as channels, the structure reported here circumferences the inherent doping nonuniformity issues in NWs grown by the vapor–liquid–solid mechanism, and self-aligned lateral epitaxy nature of our NW structure makes scaling up to NW array-based transistors from the bottom up feasible.**

***Index Terms*—GaAs, high-electron-mobility transistors (HEMTs), nanowire, scalability, III–V.**

I. Introduction

III–V semiconductor nanowire (NW) field-effect transistors (FETs) (NW-FETs) have attracted a lot of attention for next-generation low-power high-speed digital and RF integrated circuit applications [1], [2]. The inherent 3-D cross section of NWs enables multigate architecture, which increases the electrostatic control of channels and thus suppresses short-channel effects. The NW geometry can also increase drain current and transconductance (G_m) since the 3-D structure increases the surface area to provide inversion channel. Bottom-up-grown self-assembled NWs are particularly interesting because of the simplicity in processing, which does not require lithography and chemical etching, and potentially smaller feature sizes than defined by lithography.

Many types of bottom-up-grown NW-FETs have been demonstrated including NW MESFET [3], [4], MISFET [5]–[7], and HEMT [8]. However, the manufacturability of bottom-up-grown NW FETs and circuits is still in question. The main challenges of realizing these NW-based very large scale integrated circuits (VLSIs) include: controllability of NW growth direction [9] and positioning, uniformity of NW electrical property, and compatibility with planar processing.

Recently, we have developed a controlled growth method for self-aligned planar GaAs NWs, with metal–organic chemical vapor deposition (MOCVD) through gold (Au)-catalyzed vapor–liquid–solid (VLS) mechanism [10]. In contrast to conventional out-of-plane $\langle 111 \rangle$ NWs, these planar NWs grow self-aligned in the $\langle 110 \rangle$ direction on (100) substrate and $\langle 100 \rangle$ direction on (110) substrate and propagate laterally epitaxially on the surface. This is essentially selective lateral epitaxy where the spatial selectivity comes from the metal-catalyst position. The planar NWs are also free of twin defects that are often found in conventional $\langle 111 \rangle$ III–V NWs. This translates into low field electron mobility as high as GaAs epitaxial films grown at high temperature and propagated along surface normal, as demonstrated using an NW-MESFET device [4]. Unlike vertical NW-FETs and postgrowth externally aligned planar NW-FETs, self-assembled planar NW-FETs are well compatible with planar processing and can be deterministically positioned for array-based NW FETs by patterning the Au catalysts. In addition, the planar NWs can be transfer printed to any desired substrates for heterogeneous integration while maintaining not only the alignment but also the registry [10]. However, the uniformity of electrical properties of the NWs across a single wire and from wire to wire remains to be an issue for doped NW channel FET operation [11]. Even when all the growth-related doping nonuniformity issues are addressed, the discrete nature of dopants makes the statistical variation of doping in nanostructures inherently nonnegligible and circuit design tolerance of such variation a challenge.

In this letter, we report on the dc characteristics of planar NW high-electron-mobility transistors (NW-HEMTs), using intrinsic GaAs planar NWs as the conducting channel and doped $Al_xGa_{1-x}As$ film grown on top of the GaAs NWs as the carrier supply layer. Because the epitaxial growth of doped $Al_xGa_{1-x}As$ thin film is well understood and controllable both in thickness and doping concentration, electrically uniform and reproducible $Al_xGa_{1-x}As$–GaAs NW-HEMTs can be achieved. By using parallel NWs as the conducting channel with common gate and source–drain, we demonstrate the linear scalability of output current and G_m. Other performance metrics including $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio and subthreshold slope (SS) of the planar NW-HEMTs will also be discussed. To our knowledge, this is the first reported bottom-up-grown planar multiple-NW channel HEMT.

II. Experiments

Fig. 1(a) shows the schematic cross section of a planar AlGaAs–GaAs NW-HEMT device structure. The planar

Manuscript received May 10, 2011; revised June 10, 2011; accepted June 14, 2011. Date of publication July 18, 2011; date of current version August 24, 2011. This work was supported in part by DARPA YFA under Grant N66001-09-1-2107 and in part by NSF awards 1001928 (ECCS) and 0749028 (CMMI). The review of this letter was arranged by Editor J. A. del Alamo.

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Digital Object Identifier 10.1109/LED.2011.2160248

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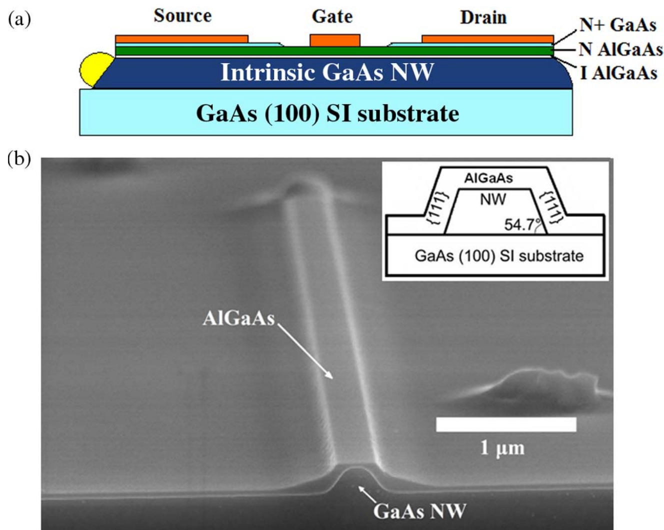

Fig. 1. (a) Schematic illustration of a planar AlGaAs–GaAs NW-HEMT structure with all the corresponding layers and metal contacts. (b) Tilted SEM image of a planar GaAs NW uniformly covered with a ∼45-nm $Al_{0.35}Ga_{0.65}As$ film. The Au catalyst particle is at the far end. The planar GaAs NW core and AlGaAs shell structure are confirmed by the void shown at the cleaved end (front) where the GaAs NW is selectively etched by citric acid : H_2O_2 (4 : 1). Inset shows the schematic cross section with crystal facets labeled. The width of the GaAs NW top facet is ∼140 nm, and the length of each side facet is ∼155 nm.

NW-HEMT structure was grown monolithically in an Aixtron 200 MOCVD reactor using TMGa, TMAl, AsH_3, and Si_2H_6 as precursors for Ga, Al, As, and Si. Au colloids of 20–250 nm diameter were randomly dispersed on GaAs surface before loading the substrates in the MOCVD reactor. Detailed growth procedure for the planar GaAs NW has been described in detail previously [10]. Planar GaAs NWs were first grown under atmospheric pressure at 460 °C using Au-catalyzed VLS mechanism on semi-insulating GaAs (100) substrates with a growth rate of ∼68 nm/s. The reactor pressure was then lowered to 100 mbar, and the growth temperature was raised to 680 °C to switch from VLS NW growth mode (through Au) to epitaxial thin-film growth mode for the AlGaAs shell deposition (Au stays at the end of the NW and elevates to the top of the surface under this condition). Specifically, 3-nm undoped $Al_{0.35}Ga_{0.65}As$ was grown as spacer directly on the GaAs planar NW top facets and sidewalls, followed by 42-nm Si-doped ($2 \cdot 10^{18}$ cm^{-3}) $Al_{0.35}Ga_{0.65}As$ as the electron supply layer. Finally, 5-nm n^+ doped ($>$ 2e18 cm^{-3}) GaAs thin film was grown to cap the AlGaAs layer and serve as source and drain ohmic contact layer. Si doping levels in AlGaAs were calibrated separately using standard planar thin-film growth. Fabrication was done using conventional optical lithography. Source and drain metal deposition was done right after growth using evaporated Ge/Au/Ni/Au (20 nm/50 nm/30 nm/50 nm) stack followed by annealing at 400 °C for 15 s. Gate recess was done by selectively etching off the n^+ GaAs layer over $Al_{0.35}Ga_{0.65}As$ using citric acid : H_2O_2 (4 : 1). Ti/Au (10 nm/140 nm) gate metal was evaporated thereafter without annealing. Mesa isolation or ion-implantation isolation step was not used.

The cross section of the planar GaAs NW is trapezoidal with {111A} sidewall and (100) top facets, as schematically shown in the inset in Fig. 1(b). Note that the entire periphery of the GaAs NW (i.e., the width of the top facet plus the two side facets) is ∼450 nm, which is used as the channel width. Care must be taken to ensure good interface quality between the faceted GaAs NW and the AlGaAs shell, which determines the density of the 2-D electron gas (2-DEG) for HEMT operation. Taking advantage of the planarity and the epitaxial nature of the NWs, we have cleaved the GaAs substrate normal to the NW axial direction, to show the cross section of the NW-HEMT structure. Citric acid : H_2O_2 (4 : 1) was used to reveal contrast between the $Al_{0.35}Ga_{0.65}As$ thin-film shell and the GaAs NW. As shown in Fig. 1(b), a void created from the removed GaAs NW can be clearly seen underneath the top $Al_{0.35}Ga_{0.65}As$ layer which conforms to the crystal facet of the GaAs NW.

III. Results and Discussion

Fig. 2(a)–(c) shows SEM images of three fully processed AlGaAs–GaAs planar NW-HEMT devices that consist of single, double, and triple NWs as conducting channels, respectively. Gate metal contact conforms to the trapezoidal shape of the NWs uniformly while source and drain appear more flat due to annealing. The separation between source and drain is 5 μm, and the gate length is ∼1 μm. These NWs are of the same dimension and perfectly parallel to each other owing to their self-alignment to $\langle 110 \rangle$ crystal direction, so that electrical characteristics should scale linearly as long as the electrical and geometrical uniformity from NW to NW is granted.

Fig. 3(a) shows the measured source-to-drain two-terminal I–V curves for three individual devices similar to those shown in Fig. 2 before gate metal deposition. The current increases linearly with voltage before reaching saturation, as reported before [4]. Noticeably, the current level scales almost exactly with the number of NWs in the channel. Fig. 3(b) shows the output characteristics of the single, double, and triple channel planar NW-HEMTs for $V_{gs} = -1.5$ to 0.5 V in steps of 0.5 V. Well-defined linear and saturation regions are observed for all devices, with a maximum output current of ∼100 mA/mm at $V_{gs} = 1$ V when normalized to the channel width (the entire periphery of NWs in channel) for the three devices, respectively. It is evident that the output current scales well as a function of number of NWs in the channel of the three-terminal devices. Fig. 3(c) shows the transfer characteristics of all three devices, which show a clear threshold operating in depletion mode. The threshold voltage -1.5 V is consistent with the layer thickness and doping levels in the structure. For each device, a group of three curves with drain voltage ranges from 1.5 to 2.5 V in steps of 0.5 V. At 1.5-V drain bias, I_{ds} starts to roll off at $V_{gs} \sim 1.5$ V probably due to the gate leakage. Extrinsic peak transconductances $G_{m,\text{ext}}$ are 83, 84, and 86 mS/mm at 2.5-V drain bias for the single, double, and triple NW channel devices, respectively. Source resistance of 8.13 $\Omega \cdot$ mm is extracted from two-terminal source-to-drain characteristics shown in Fig. 3(a). The huge source resistance is probably due to the thin GaAs cap, thick $Al_{0.35}Ga_{0.65}As$ barrier layer, and large gate-to-source distance, which holds large room for improvement. Intrinsic peak transconductances $G_{m,\text{int}}$ of 255, 265, and 286 mS/mm are estimated for the single, double, and triple NW channel devices, respectively. I_{ON}/I_{OFF} for all devices is $\sim 10^4$ as shown in the inset in Fig. 3(c), and SS is in the range of 119–181 mV/dec. Both I_{ON}/I_{OFF} and SS can be readily improved using mesa etching or ion implantation

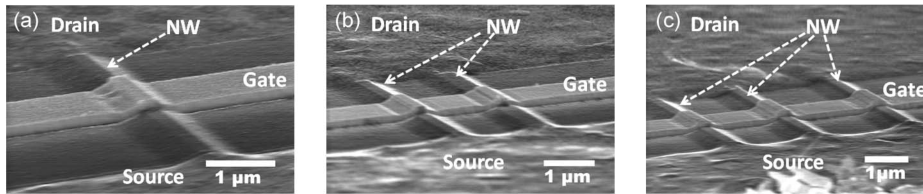

Fig. 2. SEM images of three fully fabricated AlGaAs–GaAs planar NW-HEMT with (a) single, (b) double, and (c) triple parallel NWs in the channel, respectively. All NWs are of the same dimension as the one shown in Fig. 1(b). The scale bar represents 1 μm.

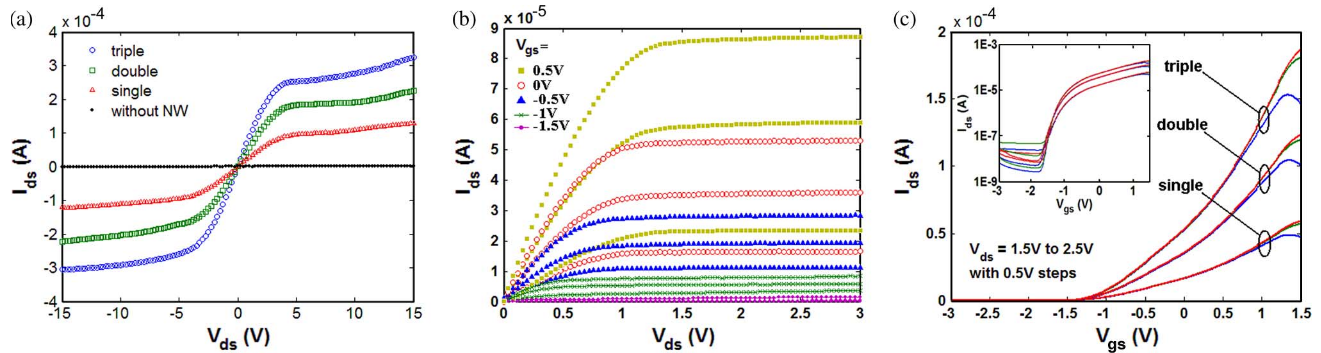

Fig. 3. DC characteristics of three AlGaAs–GaAs planar NW-HEMTs with single, double, and triple NWs in the channels. (a) Two-terminal source-to-drain I–V curves before gate deposition for single, double, and triple NWs. (b) Output characteristics for $V_{\rm gs} = -1.5$ to 0.5 V in steps of 0.5 V. Each set of color-coded curves represent the data taken from devices with (bottom) single, (middle) double, and (top) triple NWs in the channel at the indicated $V_{\rm gs}$. (c) $I_{\rm ds}$–$V_{\rm gs}$ transfer characteristics for $V_{\rm ds} = 1.5$ to 2.5 V in steps of 0.5 V; Inset shows $I_{\rm ds}$–$V_{\rm gs}$ plot on a semilog scale. The gate length is $\sim$ 1 μm, and the channel length is 5 μm for all devices.

TABLE I
DC PERFORMANCE OF AlGaAs–GaAs PLANAR MULTIPLE-NW CHANNEL HEMTs

# of NWs in the channel	Single	Double	Triple
drive current (mA/mm) (at V_{gs}=1V)	100	102	102
peak $G_{m,ext}$ (mS/mm) (at V_{ds}=2.5V)	83	84	86
peak $G_{m,int}$ (mS/mm) (at V_{ds}=2.5V)	255	265	286
V_T (V)	-1.5	-1.5	-1.5
SS (mV/dec)	181	173	119
I_{ON}/I_{OFF}	10^4	10^4	10^4

isolation. Table I summarizes all the dc performance metrics of the planar multiple-NW channel HEMTs. The slight differences in peak G_m, as well as output current among three devices, are attributed to processing-related variations of gate length. The excellent linear scalability demonstrated here will enable planar NW array-based HEMTs with high output current.

IV. CONCLUSION

In conclusion, we have reported the first bottom-up planar NW-HEMT with monolithically grown multiple GaAs NW channel and doped AlGaAs shell operating in depletion mode. The demonstrated NW-HEMTs have excellent, uniform, and scalable dc characteristics. With NW size scaling, improved schemes for better source and drain contacts, self-aligned short-channel processing, and reduced gate leakage by depositing gate dielectric, the device performance is promising to surpass its planar counterpart. Taking advantage of the distinctly small width/length ratio of NW channel, enhanced gate controllability, low leakage current, high electron mobility, and versatile drive current levels through the use of different number of NWs in the channel, high-speed low-power mixed signal circuits can be built out of this planar NW-FET technology. RF performance of planar NW-HEMTs using small NWs is being studied and will be reported separately.

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