

Nanoscale three dimensional pattern formation in light emitting porous silicon

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A simple and efficient method for generating light emitting three-dimensional (3D) nanoscale pattern in silicon is presented. The method is based on differential chemical etching on and in-between patterned metal features. Effective transfer of various two-dimensional nanoscale (10–100 nm) metal patterns on bulk silicon to 3D porous silicon network is demonstrated. The capability and limitations of this method are discussed. © 2008 American Institute of Physics.
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Porous silicon remains to be an interesting focus of research, largely due to its light emitting property in contrast to its bulk counterpart, the large surface to volume ratio for sensing applications, its structural compliance for epitaxial growth, and the periodicity for photonic crystal applications. Porous silicon itself is a nanostructured material consisting of interconnected crystallites that are of the dimension of 1–50 nm. Patterned porous silicon structures are potentially useful for integrated optical and sensing systems. Promising approaches for micron and submicron scale pattern formation have been reported, using either lithography methods which selectively masks the porous silicon removal or generation, or maskless localized treatment of silicon surface which blocks or enhances porous silicon formation or dissolution. Specific techniques used include ion irradiation or implantation,^{1–4} electron beam lithography and irradiation,^{5,6} localized far-field or near-field illumination,^{7,8} dry-removal soft lithography,⁹ and lithography with multilayer electrochemical resistant mask.² The spatial resolution of these techniques is limited by lithography tools or the well-known fragility and reactivity during porous silicon formation or etching.^{5,10} As a result, a nanoscale (<100 nm) large area fabrication method for patterned porous silicon is still lacking.

A simple, fast, and effective porous semiconductor formation method, where etching was assisted by metal without external bias, was reported by Li and co-workers.^{11,12} In contrast to the conventional way of producing porous silicon where external bias is applied to drive holes (h^+) for semiconductor dissolution, metal assisted porous silicon formation occurs at open circuit. In addition to the simplicity, metal-assisted chemical etching allows patterned porous silicon to be formed, because etching proceeds differently on and off the metal and for different substrate doping types and levels.^{11,13} Micron to submillimeter size features^{14–16} in porous silicon have been recently demonstrated using metal-assisted chemical etching. It is important to note that the metal in this method does not act as a mask, rather as a catalyst for hole (h^+) generation for semiconductor dissolution. We demonstrate here true nanoscale three dimensional

(3D) patterns in light emitting porous silicon, transferred from two-dimensional (2D) metal nanopatterns in less than 1 min etching time, with controlled topography and luminescence properties.

Various nanoscale patterns, including dot, mesh, lines, grids, boomerang contour arrays in the range of 10–100 nm in dimension, were written on polymethyl methacrylate on *p*-type (100) Si substrates (7 Ω cm), using electron beam lithography at 50 kV. Platinum (Pt) and Titanium (Ti) metals were evaporated and followed with standard lift-off. Metal patterned substrates were then etched in the H₂O₂ metal-HF (HOME-HF) etchant¹¹ for 15–90 s. Morphology resulted from etching was examined with scanning electron microscope (SEM) and atomic force microscope (AFM). Optical properties of the etched samples were characterized using photoluminescence (PL) spectroscopy pumped by the 514 nm line of an argon laser and cathodoluminescence (CL) imaging.

Shown in Fig. 1(a) is a SEM image of an array of Ti/Pt dots with height of 15 nm (5 nm Ti followed by 10 nm Pt), diameter of 15 nm, and pitch of 100 nm patterned on a *p*-type silicon substrate. Figure 1(b) shows the pattern after 30 s etching in HOME-HF solution. It can be seen that indentations are formed where the Ti/Pt dots were, while uniform porous structures (see inset for close up image) were formed around the dots. The depth of the indentations was estimated to be on the order of 60 nm by measuring the cross section of an array of adjacent line patterns.

Room temperature PL measurement was performed on a variety of patterned porous silicon structures to confirm the light emitting nature of the porous silicon thus produced.

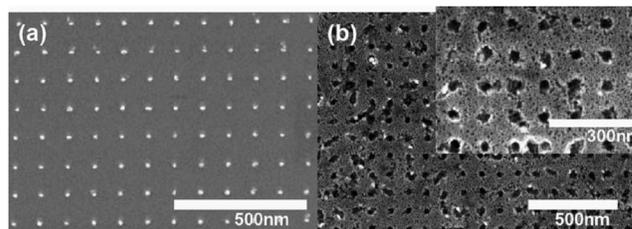


FIG. 1. SEM images of an array of 15 nm Ti/Pt dots before (a) and after 30 s etching (b). Inset at upper right shows close up image of the after etching porous structure.

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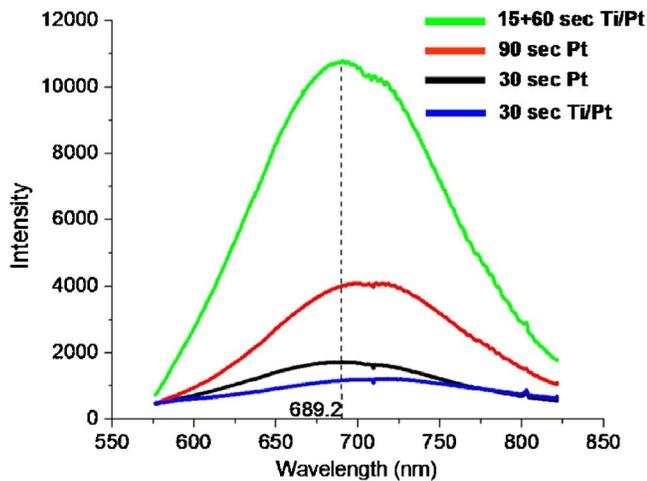


FIG. 2. (Color online) A series of PL spectra from the dot patterned samples after development at the specified conditions.

Displayed in Fig. 2 is a set of PL spectra taken from dot patterned samples at specified conditions. The intensity varied with etching time in general. However, the wavelengths remained around 700 nm for the range of etching time studied. Red emission is visible to naked eyes under UV lamp illumination, which is remarkable considering the emission depth (~ 60 nm) and area ($44 \times 44 \mu\text{m}^2$).

When the metal pattern was reversed from dot to mesh (i.e., a continuous Ti/Pt sheet with circular blanks), arrays of pillars were formed where the Ti/Pt mesh voids were located, as shown in Fig. 3. The pillars are porous in structure and are of the same size as the mesh voids. It can be clearly seen from Fig. 3(b) that the height difference between the pillars [flush with the starting material shown at the right side of Fig. 3(b)] and their surrounding results from the depression in height from areas covered with the Ti/Pt sheet.

In order to characterize the topography and uniformity in detail, lithographic metal patterns of relatively large dimensions (still < 100 nm) are studied. Shown in Fig. 4(a) are as deposited Ti/Pt contour patterns on a *p*-type silicon substrate, with the boomerang-shaped arm width at 80 nm and a pitch of $1 \mu\text{m}$ between the square contours. Figure 4(b) shows the SEM image after the pattern was developed in the etching solution for 30 s. A 3D view of an AFM surface topology of this developed pattern is shown in Fig. 4(c). As materials underneath the metal are removed, the metal appears to conform well to the recessed semiconductor surface, and becomes engraved in the silicon body at the bottom of the trench. AFM line scans over features before and after pattern development show that the as-patterned metal height is only ~ 11 nm, while the metal pattern after development

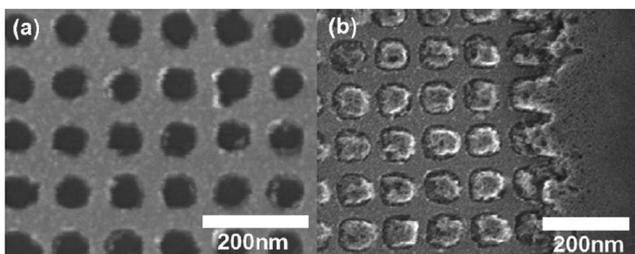


FIG. 3. SEM images of a sheet of Ti/Pt with ~ 70 nm size voids before (a) and after 30 s etching (b).

became deep trenches with an average depth of ~ 100 nm and a standard deviation of 15 nm. This variation may be related to the imperfect conformities of boomerang patterns to the receding surface. Similar to the dot and mesh patterns, the areas in-between metal features are light emitting silicon with fine pores (high resolution SEM image not shown). The light emitting nature is demonstrated in Fig. 4(d) from a CL panchromatic image, where the high intensity luminescent locations (lighter in color) correspond to areas in between the metal lines. In previous reports on metal-assisted micron to submillimeter scale porous silicon patterning, however, light emission appeared to originate right at and immediately around where metal was deposited.^{14,16} This difference could be related to dimensionality but may also result from the metal deposition method or annealing schemes used.

Interestingly, in areas where the metal peels off and the surface underneath is revealed, SEM [Fig. 4(e)] shows distinct porous features in that region also, but the pore size is much bigger than that of the surrounding areas (areas without metal coverage). This is consistent with the macroscopic metal-assisted porous silicon formation behavior on and off metal for *p*-type silicon,¹¹ where faster etching directly underneath the metal produces larger pores that are deeper while finer pores that are shallower in depth are generated in the surrounding areas. However, the top surface remains planar for patterns of millimeter scale.^{11,13} For the nanoscale patterns studied here (10–100 nm), the fast etch rate under the metal leads to not only larger pores but material removal (electropolishing), which results in 3D nanoscale structures.

In all metal features including dot, mesh, parallel lines, and boomerang contours discussed above, a 2D metal pattern on planar silicon surface has clearly been transferred into a 3D patterned porous silicon network. In the following, we discuss the limitation and capability of this method. It can be seen from Fig. 1(b) that the size of the indentations in the developed pattern are of slightly larger diameters and with some irregularities, compared to the original size of Ti/Pt dots. This can be attributed to the insufficient adhesion of metal dots to silicon surface during the etching process where H_2 gas is generated. For the reverse pattern using metal mesh [Fig. 3(b)], the metal sheet does not seem to be laterally mobile. However, the fragility of the resulted thin porous pillars limits the spatial resolution and aspect ratio of such structures. In the case of the boomerang contour patterns in Fig. 4, the pattern transfer fidelity is apparently better due to the larger feature size and thus better stability of the metal spatial adherence. In general, the 2D to 3D pattern transfer fidelity and resolution limit are dependent on how well the patterned metal features form a coherent interface with the semiconductor during pattern development, which can be affected by metal feature length and width, as well as etching rate. This is especially important for high aspect ratio patterns where longer etch time is required.

As long as metal features maintain their spatial placement during pattern development, the lateral boundary between the metal and silicon seems to be well defined using this method. The SEM image in Fig. 4(f) shows the interface between a near vertical porous silicon sidewall and the engraved metal line. Since metal-assisted etching is initiated by hole (h^+) generation at the metal catalyst,¹¹ the distinct boundary shown in Fig. 4(f) indicates that holes generated at the metal catalyst remain largely confined and consumed underneath the metal, even when the metal features are spaced

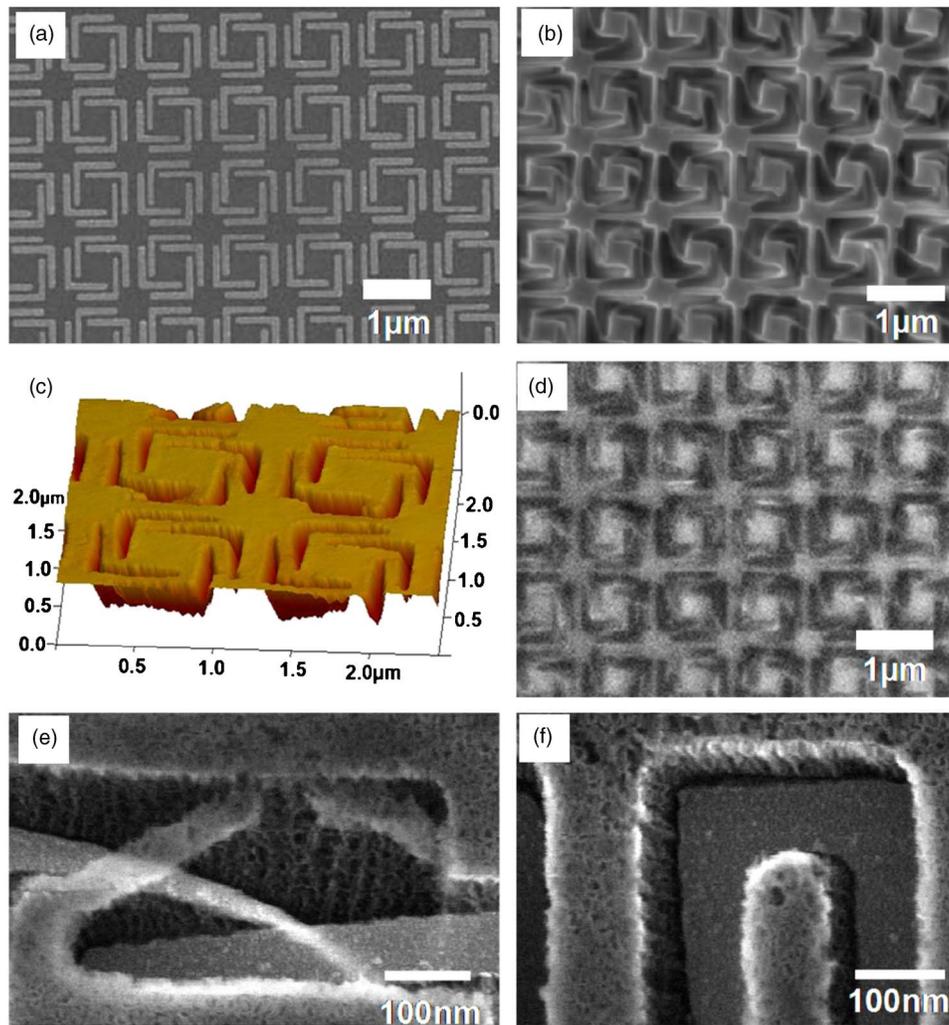


FIG. 4. (Color online) (a) SEM image of as deposited Ti/Pt metal boomerang contour pattern. (b) SEM image (taken at high beam current) of pattern in (a) after 30 s etching development. (c) Cross-sectional AFM image showing the 3D nature of the developed patterns. (d) Panchromatic CL image of pattern in (b) taken at the same beam current as in (b). (e) High resolution SEM revealing the porous structure underneath the metal. (f) High resolution SEM image of a linear trench pattern showing the vertical sidewall and the distinct boundary between engraved metal and porous silicon.

less than 100 nm apart. Note that this spacing is several orders of magnitude smaller than the typical hole diffusion length in *p*-type silicon. This implies that the hole consumption (etching) rate is much faster than the hole diffusion rate. Since the reaction front continues to move downward as the materials are removed underneath the metal, 3D nanofeatures fabricated using this method do not show undercut, in contrast to making patterned porous silicon using photoresist or e-beam resist as mask.¹⁰

In conclusion, a simple and efficient method has been presented to form nanoscale (10–100 nm) 3D patterns in light emitting porous silicon. In this method, nanoscale metal pattern is used to assist differential chemical etching under and in-between metals. Material removal occurs directly underneath the metal due to the fast catalytic etching reaction. This results in the imprint of the 2D lithography metal pattern into 3D silicon body. Due to the nature of the pattern development process, porous silicon formation is achieved in the same step and a 3D nanoscale patterned porous silicon structure with vertical sidewalls can be generated. For high fidelity pattern development, it is critical to ensure metal patterns not to lift-off during etching by increasing metal adhesion and controlling the chemical etching condition, especially for small high aspect ratio dimensions. This nanos-

cale fabrication method, with modification, is expected to be applicable to other semiconductor materials.

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