Planar GaAs nanowire tri-gate MOSFETs by vapor–liquid–solid growth

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Abstract
Depletion-mode metal–oxide–semiconductor field effect transistors (MOSFETs) with GaAs planar nanowire (NW) channels are successfully demonstrated. The Si-doped planar GaAs NWs are grown in a selective lateral epitaxy manner via Au-assisted vapor–liquid–solid (VLS) mechanism. A SiO2 interlayer between the multi-faceted NW and Al2O3 high-k dielectric formed by atomic layer deposition (ALD) improves the NW MOSFET performance.

1. Introduction
III–V semiconductor nanowires (NWs) have received much attention recently due to their high intrinsic electron mobility and the inherent 3-dimensional geometry which facilitates the realization of multi-gate transistors [1]. Comparing with top–down approaches, bottom–up vapor–liquid–solid (VLS) growth method is of particular interest since it produces NWs with smooth facets that are free of etching damage. However, conventional VLS NWs grow out of the substrate plane, which makes them incompatible with the well-established planar processing technology and thus prevents them from entering practical electronic applications readily [2]. To address this issue, our group has recently developed a controlled VLS growth method to assemble planar and self-aligned GaAs NWs by metalorganic chemical vapor deposition (MOCVD) [3]. Unlike the out-of-plane NWs, planar NWs are grown laterally and propagate in parallel along ⟨110⟩ and ⟨100⟩ directions on ⟨100⟩ and ⟨111⟩A substrates, respectively [4]. The planar geometry and self-aligned nature are very attractive in terms of device integration. The epitaxially smooth multi-faceted cross-section profile makes these planar NWs ideal for multi-gate FETs [3–5]. So far high-performance MESFET and HEMT devices have been demonstrated using such planar NWs as the conduction channels [3,6]. In this letter, we further demonstrate planar NW functionality by the successful realization of depletion-mode MOSFETs based on Si-doped n-type planar GaAs NWs using Al2O3 as the gate oxide. For III–V multi-gate transistors, simultaneous passivation of different crystal facets could be challenging since interface trap density has strong crystal orientation dependence [7]. We here use SiO2 deposited by plasma-enhanced chemical vapor deposition (PECVD) as an interfacial layer between Al2O3 and the GaAs NW surface to further improve the interface quality and device performance [8].

2. Growth and fabrication
GaAs planar NWs were grown on (100) semi-insulating GaAs substrate by atmospheric pressure MOCVD at 460 °C utilizing colloidal Au particles (250 nm in diameter) as growth catalysts. Si2H6 was used as the n-type doping precursor. The NWs, trapezoidal in cross-section, have a bottom width of ~280 nm. Top surface has been identified to be (100) whereas the two sidewalls are (111)A [3,4]. Standard Ge/Au/Ni/Au metal stack is used for S/D contact whereas Ni/Au is used for gate contact. The gate length is measured to be ~850 nm. The nominal thickness for the MOSFET high-k Al2O3 layer is 7.2 nm. When an interfacial layer of ~1 nm was inserted between the multi-faceted GaAs NW and the high-k Al2O3 layer, the Al2O3 thickness was reduced accordingly to 6.3 nm.

For capacitance–voltage (C–V) measurements, MOS capacitors (MOSCAPs) were fabricated on commercial n-type doped (1–3 × 1016 cm−3) GaAs (100) substrates. (100) surface is known to have strong Fermi level pinning due to high interface trap density whereas (1 1 1)A is inherently unpinned [7].

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3. Results and discussion

Fig. 1(a) shows the C–V curves of an n-type GaAs MOSCAP with 10 nm Al₂O₃. Very large frequency dispersion (0.11 µF cm⁻²/dec at Vₕ = 3 V) is observed, indicating poor interface quality [7]. We attempted to deposit an amorphous silicon interlayer between ALD Al₂O₃ and GaAs by PECVD to improve the interface quality, following [8]. Indeed, much less frequency dispersion (0.024 µF cm⁻²/dec at Vₕ = 3 V) is observed as shown in Fig. 1(b). However, the as-deposited material was actually SiO₂ because of the residual oxygen in our PECVD chamber. This is confirmed by the fact that the material cannot be etched by XeF₂ and the refractive index measured from calibration samples by ellipsometry is 1.44. Never the less, substantial improvement of C–V characteristics can be achieved by using this SiO₂ interlayer as shown in Fig. 1(b). It is likely that the same mechanism as discussed in Ref. [8] applies here since the GaAs–Si interface chemistry should still be the same under the dominantly Si-rich PECVD environment.

A SEM image of a fabricated GaAs NW MOSFET is shown in Fig. 2. The inset shows the trapezoidal cross-section profile of the NW channel with a (1 0 0) top facet and two (1 1 1)A side facets, a tri-gate structure. The output characteristics of the device with the interlayer are shown in Fig. 3. Fig. 4(a) shows the comparison of sub-threshold characteristics between the devices with and without SiO₂ interlayer. V₉ᵢ varies from 0.5 V to 1.5 V with 0.5 V step for both devices. The sub-threshold slope of the device without the interlayer is calculated to be 190 mV/dec whereas a better value of 160 mV/dec is obtained for the one with the interlayer. The drain-induced barrier lowering (DIBL) is measured to be 150 mV/V for both devices. Also shown in Fig. 4(a) is the gate leakage current measured at V₉ᵢ = 0.5 V. Note that the transfer curves of the device with interlayer are shifted toward right by 0.5 V in order to ensure clarity. (b) Comparison of on-state transfer characteristics between devices with and without interlayer at V₉ᵢ = 2 V.

Fig. 1. C–V measurement results of Al₂O₃/GaAs n-type MOSCAPs without (a) and with the SiO₂ interlayer (b).

Fig. 2. Top-view SEM image of a fabricated planar NW MOSFET device. The scale bar represents 4 µm. The inset SEM image shows the cross section of an as-grown planar NW with a (1 0 0) top facet and two (1 1 1)A sidewalls [4]. The scale bar in the inset represents 80 nm.

Fig. 3. Output curves of the Planar NW MOSFET device with the SiO₂ interlayer.

Fig. 4. (a) Comparison of sub-threshold and gate leakage characteristics between devices with and without the interlayer. V₉ᵢ varies from 0.5 V to 1.5 V with 0.5 V step for transfer curves of both devices. The gate leakage current is measured at V₉ᵢ = 0.5 V. Note that the transfer curves of the device with interlayer are shifted toward right by 0.5 V in order to ensure clarity. (b) Comparison of on-state transfer characteristics between devices with and without interlayer at V₉ᵢ = 2 V.
extrinsic $g_m$ is about 73 mS/mm for the device with the interlayer. The intrinsic $g_m$ is estimated to be about 92 mS/mm by taking into account the source-side series resistance (2.8 kΩ μm by estimation). These numbers are comparable to the transconductance achieved on thin-film depletion-mode GaAs MOSFETs [9]. For the device without the interlayer, $g_m$ is lower in general and quickly rolls off after the gate voltage reaches ~1 V beyond threshold. The comparison in Fig. 4 indicates that the NW surface Fermi level can be more effectively moved in the device with the interlayer. In addition, we observe a double-hump feature in the $g_m$ curve of the device without interlayer, which is presumably related to the presence of two kinds of facets in our planar NW. This feature is seen to be removed (Fig. 4(b)) by applying the interlayer which can improve passivation quality of top (100) facet (Fig. 1), the worse one of the two.

4. Conclusion

In conclusion, we have demonstrated planar GaAs NW MOSFETs, which is yet another type of FET successfully achieved after MESFETs and HEMTs using the MOCVD grown, epitaxially smooth and multi-faceted, planar NW platform. A SiO$_2$ interfacial layer, inserted between GaAs NW and high-$k$ Al$_2$O$_3$ dielectric, improves the interface quality and device performance. The growth of ultrathin planar NW with Indium-containing high electron mobility III–V materials, which are of more interest for digital and RF applications, is currently under study.

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References