

TOPICAL REVIEW

Metal-catalyzed semiconductor nanowires: a review on the control of growth directions

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Online at stacks.iop.org/SST/25/024005**Abstract**

Semiconductor nanowires have become an important building block for nanotechnology. The growth of semiconductor nanowires using a metal catalyst via the vapor–liquid–solid (VLS) or vapor–solid–solid (VSS) mechanism has yielded growth directions in $\langle 111 \rangle$, $\langle 100 \rangle$ and $\langle 110 \rangle$ etc. In this paper, we summarize and discuss a broad range of factors that affect the growth direction of VLS or VSS grown epitaxial semiconductor nanowires, providing an indexed glimpse of the control of nanowire growth directions and thus the mechanical, electrical and optical properties associated with the crystal orientation. The prospect of using planar nanowires for large area planar processing toward future nanowire array-based nanoelectronics and photonic applications is discussed.

1. Introduction

Semiconductor nanowires have garnered much attention over the past several years as promising nanotechnology building blocks that are expected to have a wide range of applications in areas such as photonics [1], electronics [2], nanoelectromechanical systems (NEMS) [3, 4] and the life sciences [5]. The bottom-up approach to nanowire growth using a metal catalyst has enabled the routine fabrication of sophisticated 1D devices that is otherwise not possible with conventional top-down approaches. This growth method is most frequently described through the vapor–liquid–solid (VLS) mechanism first described by Wagner and Ellis with silicon whiskers grown with a gold (Au) catalyst [6]. A liquid metal particle heated in the presence of semiconductor gas precursors acts as a preferential sink to collect material from the surrounding vapor reactants. The metal particle then becomes supersaturated and will precipitate the collected material in the form of a 1D semiconductor nanowire with a diameter similar to the size of the metal particle. Further growth and extension of the nanowire occur when an additional material precipitates onto the interface between the metal

particle and the nanowire. The growth of nanowires generally occurs above the eutectic temperature of the metal catalyst and the semiconductor material, although a vapor–solid–solid (VSS) mechanism where the growth temperature is below the eutectic temperature and the metal catalyst is thought to be solid has also been used to describe nanowire growth [7, 8]. Nanowires have been grown using several different kinds of techniques including chemical vapor deposition (CVD) [9, 10], laser ablation [11], supercritical fluid solution phase [12], metalorganic chemical vapor deposition (MOCVD) [13–15], chemical beam epitaxy (CBE) [16, 17] and molecular beam epitaxy (MBE) [18, 19].

The VLS mechanism has proven to be extremely flexible and allows for the controlled growth of complex nanostructures. For example, heterojunctions can be formed axially along the nanowire simply by modifying the material precursors present in the reaction chamber [13, 20–23]. Radial heterojunctions can instead be formed if the reaction temperature is increased to suppress the VLS growth and enhance deposition of material on the sidewalls of the nanowire [24]. Axial and radial impurity doping for both n-type and p-type materials can be achieved by adding a suitable

Table 1. Commonly observed growth directions and cross-sections (if known) for several important semiconductor nanowires. The listed references are not exhaustive; only a few representative references are cited in the table.

Material	Growth directions	Nanowire cross-sectional geometry (if known)	Notes	References
Si	$\langle 111 \rangle^a$	See [50]	>20 nm diameter	[6, 10, 51, 52]
	$\langle 110 \rangle^a$	See [50]	<20 nm diameter	[10, 12, 52, 53]
	$\langle 112 \rangle^a$		<20 nm diameter	[53, 54]
	$\langle 100 \rangle$	See [50]		[12, 55]
Ge	$\langle 111 \rangle^a$			See [56] for the comprehensive list
	$\langle 110 \rangle^a$			
	$\langle 112 \rangle^a$			
GaAs	$\langle 111 \rangle B^a / [0001]^{a,b}$		Often polytypic (ZB/WZ) with stacking faults	[45]
	$\langle 110 \rangle$		No stacking faults, lateral growth on (001) GaAs surface	[57, 58, 59]
	$\langle 110 \rangle$		No stacking faults	[19]
	$\langle 112 \rangle$			[60]
	$\langle 100 \rangle$		Si (111) substrate, no stacking faults	[61]
	$\langle 111 \rangle A$		No stacking faults	[62]
InP	$\langle 111 \rangle B^a / [0001]^{a,b}$		Often polytypic (ZB/WZ) with stacking faults	[63]
	$\langle 110 \rangle$			[64]
	$\langle 100 \rangle$		No stacking faults	[65]
InAs	$\langle 111 \rangle B^a / [0001]^{a,b}$		Often polytypic (ZB/WZ) with stacking faults	[45]
	$\langle 100 \rangle$			[14]
	$\langle 110 \rangle$		Lateral growth on the InAs (001) surface	[14]
	$\langle 112 \rangle$		Lateral growth on the GaAs (111)B surface	[66]
ZnO ^b	$[0001]^a$			[34, 67, 68, 69]
	$\langle 10-10 \rangle$ <i>m</i> -axis		Aligned lateral growth on <i>a</i> -plane sapphire	[70]
GaN ^b	$[0001]$ <i>c</i> -axis		Polar direction	[47, 71, 72, 73]
	$\langle 10-10 \rangle$ <i>m</i> -axis		Nonpolar direction	[11, 47, 74, 75]
	$\langle 11-20 \rangle$ <i>a</i> -axis		Nonpolar direction	[73, 75, 76]

^a Indicates most commonly observed growth directions.

^b Signifies the wurtzite crystal structure.

precursor [25, 26]. Nanowire heterojunctions can be highly lattice-mismatched as the induced strain can be coherently accommodated through lateral relaxation [27]. For the same reason, nanowires can be grown relatively defect-free on highly dissimilar substrate materials (e.g. III–V nanowires on Si substrates [28]) that would otherwise be extremely difficult as two-dimensional thin films. These unique properties have allowed the fabrication of a diverse range of nanowire-based devices including field-effect transistors [29–31], lasers [32–34], light-emitting diodes [35, 36, 37], photodetectors [38–40] and solar cells [41–43] among others.

Nanowires generally grow in the crystal direction that minimizes the total free energy which, in most cases, is dominated by the surface free energy of the interface between the semiconductor and the metal catalyst. For diamond and zinc-blende crystals (i.e. Si, Ge, GaAs, InP) it has been widely observed that the semiconductor–catalyst interface often forms a single surface at the lowest-energy $\langle 111 \rangle$ plane and thus nanowires tend to grow in the $\langle 111 \rangle$ direction for most growth conditions [6]. Other low-index growth directions have been occasionally reported including $\langle 001 \rangle$, $\langle 110 \rangle$ and $\langle 112 \rangle$. For compound zinc-blende semiconductors and their alloys (i.e. GaAs, GaP, InAs and InP), $\langle 111 \rangle$ directions can be further

distinguished into $\langle 111 \rangle A$ and $\langle 111 \rangle B$ depending upon the atomic layering sequence and thus surface termination. The $\langle 111 \rangle B$ (group-V terminated) is the lower energy plane [44] and therefore nanowires have been generally observed to grow in the $\langle 111 \rangle B$ direction [45]. Nanowires with a wurtzite crystal structure (e.g. ZnO, GaN) are often observed to grow along the $\langle 0001 \rangle$ direction (*c*-axis). III-nitride nanowires seem to show less preference to a particular growth orientation and growth axes perpendicular to the *a*-planes [33], *m*-planes [11, 46] and *c*-plane [47] have been observed. III–V nanowires can also form a wurtzite crystal structure or exhibit polytypism [48] switching between zinc-blende and wurtzite.

Summarized in table 1 is a list of reported nanowire growth directions for several important semiconductor materials. The control of the nanowire growth direction has several practical and technological and fundamental scientific implications. Consider for example the manufacturability of vertical arrays of nanowire field-effect transistors which are commonly fabricated by patterning the metal catalyst to grow vertically aligned $\langle 111 \rangle$ nanowires on $\langle 111 \rangle$ substrates (see for example Mårtensson *et al* [49]). Although researchers have had much success in forming small nanowire arrays, commercial logic products based on nanowires will require millions (sometimes

billions) of devices per chip. A single misgrown nanowire may be the difference between a yielding or faulty chip. From a fundamental scientific point of view, the optical, electrical and mechanical properties of nanowires are expected to differ with the growth direction and could have useful applications tailored by orientation. In particular, III–V semiconductors when grown in the $\langle 111 \rangle$ B direction often exhibit a high density of stacking faults that can degrade device optical and electrical characteristics and therefore growth in other directions (which generally result in defect-free nanowires) is of great interest.

The purpose of this paper is to provide a comprehensive review of the methods in which the nanowire growth direction can be controlled. We focus primarily on nanowires of the major semiconducting materials that are epitaxially grown with the metal-catalyzed VLS or VSS mechanism. Many factors that affect the nanowire orientations are interconnected and this paper is organized to attempt for the best clarity and coherence. We begin with a discussion about the role of the substrate in controlling the nanowire growth direction including heteroepitaxy of nanowires. The role of a nanowire diameter on growth orientation will then be reviewed followed by analysis of the various means of controlling nanowire orientation through growth conditions. We will then discuss the growth of nanowires in-plane with the growth substrate with a focus on our recent results on $\langle 110 \rangle$ planar III–V nanowires. Finally, the last section will cover nanowire branching and kinking.

2. Control of epitaxial nanowire growth orientations

2.1. Substrate crystal orientation effect

Perhaps the simplest way to engineer nanowire orientation (relative to the growth surface) is to change the crystal orientation of the substrate. Growth substrates are often chosen such that the nanowire growth direction is normal to the growth plane. For example, as discussed in the introduction, nanowires with cubic crystal structure typically grow in the $\langle 111 \rangle$ direction and therefore they are often epitaxially grown on $\langle 111 \rangle$ substrates to achieve vertically aligned, out-of-plane nanowire growth along the surface normal. In the case of compound semiconductor nanowires, $\langle 111 \rangle$ B substrates are chosen for vertically aligned $\langle 111 \rangle$ B oriented nanowires. Similarly, vertically aligned wurtzite ZnO and GaN nanowires can be grown on, for example, a -plane sapphire substrates. By patterning the metal catalyst through e-beam [49, 77, 78] or nano-imprint lithography [79] on proper substrates, it is possible to achieve extremely uniform arrays of vertical position-controlled nanowires.

Summarized in tables 2 and 3 (and illustrated schematically in figure 1) are the available out-of-plane $\langle 111 \rangle$ and $\langle 111 \rangle$ B directions for several key elemental and compound semiconductor substrates respectively. In figure 1, both the elemental and compound substrates are combined into the same schematic and the $\langle 111 \rangle$ B direction is specified by gray shading. As can be seen from figures 1(a)–(f), for nanowires grown on the $\langle 111 \rangle$ elemental substrate, the

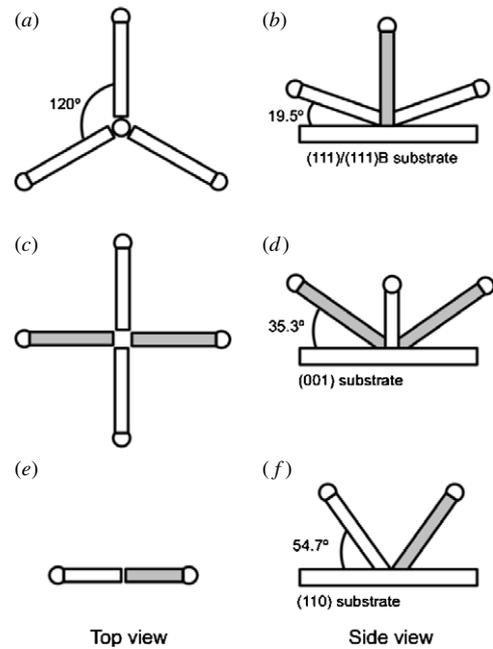


Figure 1. Schematic illustration of $\langle 111 \rangle$ nanowires grown epitaxially on several different substrate orientations. Both elemental and compound semiconductor substrates are combined into the same illustrations with $\langle 111 \rangle$ B directions specified via gray shading of the nanowire. (a), (b) $\langle 111 \rangle$ / $\langle 111 \rangle$ B substrate. (c), (d) $\langle 001 \rangle$ substrate. (e), (f) $\langle 110 \rangle$ substrate. The top view is shown in (a), (c), (e) and the side view shown in (b), (d), (f).

Table 2. Available $\langle 111 \rangle$ growth directions and their geometric relationship on several different elemental semiconductor substrate orientations.

Substrate	Number of $\langle 111 \rangle$ growth directions	Angle with respect to the substrate surface	Azimuth between nanowires
$\langle 001 \rangle$	4	35.3°	90°
$\langle 110 \rangle$	2	54.7°	180°
$\langle 111 \rangle$	4	3 directions— 19.5° 1 direction— 90°	120° n/a

Table 3. Available $\langle 111 \rangle$ B growth directions and their geometric relationship on several different compound semiconductor substrate orientations.

Substrate	Number of $\langle 111 \rangle$ B growth directions	Angle with respect to the substrate surface	Azimuth between nanowires
$\langle 001 \rangle$	2	35.3°	180°
$\langle 110 \rangle$	1	54.7°	n/a
$\langle 111 \rangle$ A	3	19.5°	120°
$\langle 111 \rangle$ B	1	90°	n/a

surface normal is actually one of four available out-of-plane $\langle 111 \rangle$ directions (the other three being angled 19.5° from the surface and azimuthally separated by 120° from each other). Nanowires generally prefer the vertical $\langle 111 \rangle$ direction, although this is not strictly true for all growth conditions and adds additional complication if only the vertical $\langle 111 \rangle$

growth direction is desired. On (001) substrates, as shown in figures 1(c)–(d), elemental semiconductor nanowires will grow in one of four out-of-plane $\langle 111 \rangle$ directions (angled 35.3° from the surface and azimuthally separated 90° from each other). Finally, on the (110) substrate there are two available $\langle 111 \rangle$ directions separated 180° from each other and angled 54.7° from the substrate surface (figures 1(e)–(f)). For nanowires grown on the (111)B compound semiconductor substrate, as shown in figures 1(a) and (b), there is only one available $\langle 111 \rangle$ B direction (the surface normal). Nanowires grow in this direction under most growth conditions; thus vertically aligned arrays of III–V nanowires are then considerably easier to fabricate. On an elemental semiconductor (001) substrate, nanowires oriented in the two available out-of-plane $\langle 111 \rangle$ B directions azimuthally separated by 180° (figures 1(c) and (d)). On the compound (110) substrate, there is only one available $\langle 111 \rangle$ B direction (figures 1(e) and (f)).

Growth of nanowires on the commodity Si substrate is of particular interest and a number of nanowire materials have been investigated such as Ge [80], GaAs [81], GaP [82] and ZnO [83]. Because of the small cross-sectional area of the interface between the Si substrate and the nanowire, many of the issues associated with heteroepitaxial growth such as lattice mismatch, antiphase domains and thermal coefficient mismatch are expected to be more easily managed. Mismatch strain between the nanowire and the substrate can be coherently relieved through lateral relaxation [27] as long as the nanowire diameter is below a certain critical diameter [84].

Heteroepitaxy of nanowires of cubic crystal structures, similar to homoepitaxy, mostly results in $\langle 111 \rangle$ or $\langle 111 \rangle$ B orientation; however, the situation is more complicated from the existence of lattice mismatch at the nanowire–substrate interface which may modify the growth direction. III–V nanowires heteroepitaxially grown on an elemental substrate such as Si can grow in any of the four chemically equivalent $\langle 111 \rangle$ substrate directions on the (111) substrate. TEM shows that Au catalyst alloys readily with the four available $\langle 111 \rangle$ facets with an out-of-plane component on the (111) Si surface [82]. A particular challenge then is controlling the growth direction such that the III–V nanowires will nucleate and only grow in the vertical $\langle 111 \rangle$ growth direction on the (111) substrate instead of the three other available angled out-of-plane $\langle 111 \rangle$ directions which are less suitable for device fabrication. Bakkens *et al* have argued that lattice mismatch at the nanowire–substrate largely determines the propensity of nanowires to grow in either the vertical or non-vertical $\langle 111 \rangle$ directions [85]. Indeed, nanowires with the largest lattice mismatch with the substrate such as InP/Si (8.1%) [28, 82] and InAs/Si (11.6%) [82] tend to grow in the non-vertical $\langle 111 \rangle$ directions. Whereas materials with minimal lattice mismatch such as GaP/Si (0.4%) [28, 82] and GaAs/Ge (0.1%) [86] can be readily grown in the vertical $\langle 111 \rangle$ direction. Materials with lattice mismatch falling between the two extremes such as InP/Ge (3.7%) [87] and GaAs/Si (4.1%) [28, 81, 82, 88] show less tendency toward any particular $\langle 111 \rangle$ direction on the (111) surface. A change in the growth direction from a vertical to non-vertical

$\langle 111 \rangle$ direction may serve as a means to relieve strain at the nanowire–substrate interface and may explain the large yield of non-vertical nanowires in highly lattice mismatched materials systems [85]. Lattice mismatch becomes less important as the diameter of the nanowire is scaled below a critical diameter that allows for strain to be relieved through lateral relaxation. Furthermore, growth surface preparation [88], thermal history [89] and initial composition of the metal catalyst [86, 90] have also been found to critically influence the growth orientation of heteroepitaxially grown nanowires and will be discussed in more detail later. Growth of nanowires in a non- $\langle 111 \rangle$ direction has also been occasionally observed with heteroepitaxial growth. Björk *et al* grew defect-free [001] InAs nanowires containing short-axial InP segments on the (111)B GaAs substrate [20]. The growth in the [001] direction was attributed to compressive strain at the InAs/GaAs interface [20]. Ihn *et al* noted the occasional growth of [001] GaAs nanowires on (111) Si substrates [61]. In both of the prior studies, the [001] nanowires were confirmed to be zinc-blende and without any stacking faults. Growth of vertically standing $\langle 110 \rangle$ Ge nanowires on GaAs (110) reported by Song *et al* was largely attributed to change in the Ga composition of the Au catalyst and nanowire [86].

Nanowires consisting of materials with wurtzite crystal structure such as ZnO and GaN have additional flexibility in that it is possible to choose a substrate that is lattice matched to either the a -plane or c -plane lattice constants provided the substrate also has similar geometrical symmetry [68]. For example, a -plane sapphire, with lattice constants $a = 4.75$ and $c = 12.94$ Å, is often chosen for epitaxial ZnO nanowire growth because of the almost exact factor of 4 between the ZnO lattice constant along the a -axis and that of sapphire along the c -axis. ZnO nanowires will then grow preferably with a [0001] orientation and maintain a nearly lattice matched epitaxial relationship with the a -plane sapphire substrate [34, 69]. Kuykendall *et al* found that it was possible to engineer the orientation and cross-section of GaN nanowires by using different substrates with similar lattice constants and symmetry of the GaN crystal structure [47]. Growth of GaN nanowires on (100) γ -LiAlO₂ substrates resulted in [1–100] nanowires with a triangular cross-section consisting of (0001) facets. Whereas on (111) MgO substrates, GaN nanowires preferred the [0001] growth direction with a hexagonal cross-section made of (10–10) planes. In both cases, the GaN nanowires grew normal to the surface. Although both types of nanowires had the wurtzite crystal structure, the photoluminescence emission spectra peak of the [1–100] nanowires was blue-shifted roughly 100 meV from the [0001] nanowires. The blue-shift was attributed to the optical property difference expected between polar [0001] and nonpolar [1–100] GaN, and possibly the modification of stress, defect incorporation and carrier confinement differences. Wang and colleagues used MOCVD to grow vertically aligned GaN nanowires in the nonpolar [11–20] direction on r -plane sapphire using the Ni catalyst [75, 91]. The [0001] GaN direction has low lattice mismatch (1.3%) with the r -plane sapphire surface and may explain the preferred [11–20] growth direction. Some nanowires were also observed to grow in the $\langle 11\bar{2}0 \rangle$ or

$\langle 10\bar{1}0 \rangle$ direction at a 30° and 60° tilt from the substrate plane, respectively [75]. The $[11\bar{2}0]$ direction may in general be preferred for GaN nanowires grown with MOCVD and Ni catalyst as Kuykendall *et al* [76] and Qian *et al* [24] also reported the growth of $[11\bar{2}0]$ GaN nanowires on *c*-plane sapphire substrates used similar apparatus and the same catalyst. Gradecak *et al* later optically pumped MOCVD grown $[11\bar{2}0]$ GaN nanowires to achieve lasing at a low threshold of 22 kW cm^{-2} ; lower than the threshold found for CVD grown $[0001]$ GaN nanowires fabricated by the same research group [33]. Lower threshold can be partly explained through consideration of the high Q-factor of the triangular cross-section (compared to hexagonal $[0001]$ nanowires) and larger optical gain along the nonpolar $[11\bar{2}0]$ direction [33, 92].

2.2. Effect of substrate surface treatment and catalyst initial condition

The growth substrate surface plays an important role in the initial nucleation of the metal catalyst and subsequent growth of a nanowire from the growth surface. As a first step to nanowire growth, a wet etch is frequently used to remove the native oxide on the growth substrate surface. For example, hydrofluoric acid can be used to remove the native oxide and hydrogen-terminate a silicon substrate surface. An *in situ* anneal step is also commonly employed before the growth of nanowires to desorb any residual native oxide or contaminants from the substrate surface. In addition, this step will allow the metal catalyst and substrate and will form the initial interfaces that will eventually become the nanowire growth front. Without proper removal of the native oxide, nanowires will grow without epitaxial relationship with the substrate and thus in a random direction relative to the surface.

Krishnamachari *et al* found that the vertical $[001]$ InP nanowire growth on InP (001) substrates was possible when the *in situ* anneal step was skipped before MOCVD nanowire growth [65]. This can be explained by the reduction of dissolution of the InP substrate into the Au catalyst without the anneal step and thus the (001) InP surface will remain intact and nucleation can form on a (001) plane and result in $[001]$ growth direction. The $[001]$ InP nanowires were found to be lacking stacking faults which resulted in a significantly higher photoluminescence intensity when compared to a $\langle 111 \rangle$ B InP nanowire [20]. It was determined and later studied in more detail [93] that the usage of the poly-L-lysine (PLL) adhesion layer was critically important in promoting $[001]$ nanowire growth. PLL is commonly used to functionalize a surface for uniform deposition of negatively charged colloidal nanoparticles. In this case PLL was deposited after colloidal Au was deposited and only the substrate surface below the Au nanoparticles was left unmodified. PLL forms a thin passivation or mask layer that inhibits crystal growth on the surface similar to selective area epitaxy, and also suppresses the thermodynamically favorable $\langle 111 \rangle$ B nanowire growth from the Au nanoparticles [93]. InAs nanowires were also observed to grow in the $[001]$ direction on the InAs (001) substrate when the anneal step was skipped [14]. Wacasar

et al showed similar results with MOCVD grown GaAs nanowires on GaAs (001) and (111) A substrates [62]. GaAs nanowires normally grow in one of two $\langle 111 \rangle$ B directions on the GaAs (001) substrate; however, when the anneal step was skipped, growth in the uncommon $\langle 111 \rangle$ A directions was also observed. When PLL was used, some GaAs nanowires were observed to grow vertically in the $\langle 111 \rangle$ A direction on a (111) A substrate. The $\langle 111 \rangle$ A nanowires were free of stacking faults and had an equilateral triangular cross-section consisting of (112) planes.

Ghosh *et al* reported recently on the influence of the surface treatment of the GaAs (001) surface prior to MBE growth of GaAs nanowires [59]. Removal of the surface oxide after UV-ozone treatment before MBE growth resulted in a high percentage of $\langle 110 \rangle$ nanowires in the plane of the substrate. This type of nanowire growth will be discussed in more detail in section 3.

The composition of the catalyst on the surface of the substrate prior to nanowire growth has also been found to influence the initial nanowire growth direction particularly in the case of dissimilar nanowire and substrate materials. Ge nanowires grown on (110) GaAs substrates reported by Song *et al* initially grew in a $\langle 111 \rangle$ direction shortly before kinking to the $\langle 110 \rangle$ growth direction [86]. Higher growth temperature leads to a more pronounced (longer) $\langle 111 \rangle$ segment. Before the nanowire growth, the Au catalyst presumably has formed a Au–Ga alloy on the surface. Thus, the initial few hundred nanometers of the Ge nanowire will contain a significant amount of Ga incorporation and may be energetically favored to grow in the $\langle 111 \rangle$ direction. As the nanowire growth continues, the Ga composition will decrease in the Ge nanowire and will switch to the $\langle 110 \rangle$ growth direction that may be more energetically favorable for a Ga-depleted catalyst. A similar kinking was observed near the base of ZnSe nanowires grown on GaAs substrates although it was largely attributed to the increased importance of nanowire surface energies as the nanowire increased in length [94].

Using a cold-wall CVD reactor, Jagannathan *et al* systematically studied the morphology of Au catalyst for different anneal conditions on Si substrates with different crystal orientations and found considerably more Au agglomeration on a (111) substrate than (100) and (110) surfaces suggesting higher Au mobility on a (111) surface [80]. Little Au agglomeration was seen for SiO_2 covered a silicon surface. Such observations show that thermal history must be considered when nanowires with a particular size or growth direction are desired (particularly Si nanowires with a diameter-dependent growth direction). Interestingly, Jagannathan *et al* also found a very low yield of nucleated Ge nanowires when the Au catalyst was annealed with argon present in the reactor instead of hydrogen [80]. This implies that lower solubility of Ge in Au under argon atmosphere compared to hydrogen, and the choice of carrier gas has an important role in VLS nanowire growth.

2.3. Diameter dependence of nanowire orientation

Silicon nanowires typically grow in the $\langle 111 \rangle$ [6] direction; however, other growth directions such as $\langle 100 \rangle$ [12, 95, 96],

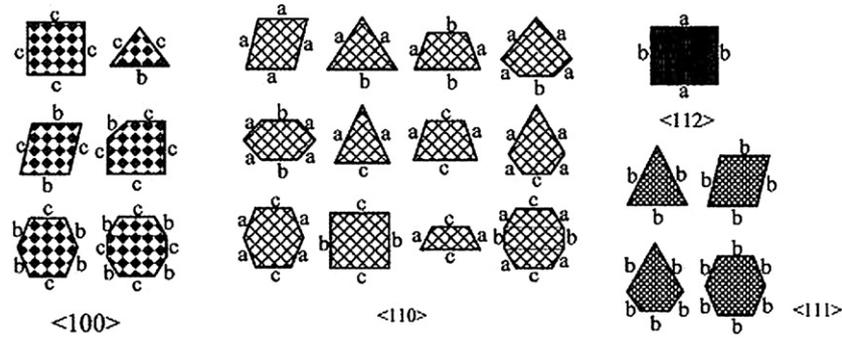


Figure 2. Possible cross-section facets of $\langle 100 \rangle$, $\langle 110 \rangle$, $\langle 111 \rangle$ and $\langle 112 \rangle$ silicon nanowires. Cross-sections with low symmetry are excluded from the diagram. The crystal planes are designated by $a = (111)$, $b = (110)$ and $c = (100)$. Adapted from [50] with permission.

$\langle 112 \rangle$ [97, 98] and $\langle 110 \rangle$ [98–100] have been commonly reported by several different research groups. It was observed by Lieber and colleagues that Au-catalyzed Si nanowires grown on SiO_2 with CVD preferentially changed the growth direction from $\langle 111 \rangle$ to $\langle 110 \rangle$ as the diameter was scaled below 20 nm [10, 53]. $\langle 112 \rangle$ nanowires were also observed and thought to represent a transitional direction between $\langle 111 \rangle$ and $\langle 110 \rangle$. This change of the growth direction can be explained by the importance of surface energetics as the diameter is scaled and the surface-to-volume ratio is increased. As mentioned above, the nanowire grows in a direction that minimizes the total free energy. Below a certain critical diameter, the free surface energy of the nanowire side facets begins to dominate and may dictate the growth direction. Lieber *et al* used cross-sectional TEM to show that the $\langle 110 \rangle$ Si nanowire side facets have a hexagonal cross-section made up of low energy (100) and (111) facets; similar to what was observed for $\langle 110 \rangle$ Si nanowires grown with the oxide-assisted growth (OAG) method. Interestingly, it was observed that the nanowire–Au interface for the $\langle 110 \rangle$ direct nanowires consisted of two (111) planes with a normal vector sum adding to the $\langle 110 \rangle$ growth direction. Wagner observed a similar interface for micron-sized $\langle 110 \rangle$ Si nanowires [101].

Schmidt *et al* confirmed that this diameter dependence also exists for epitaxial Si nanowires grown on Si (001) substrates [52]. They found excellent agreement with Lieber *et al* and observed a critical radius of approximately 20 nm below which Si nanowires transition from the $\langle 111 \rangle$ to $\langle 110 \rangle$ growth direction. Furthermore, considering only the interfacial energy of the liquid–solid interface and the surface tension of the Si nanowire, a theoretical critical radius was calculated and agreed well with experimental results.

Shown in figure 2, Zhang *et al* comprehensively studied the energetics of the possible low-index hydrogen-terminated Si nanowire cross-section surfaces and found that the low-index surface energy order was $\gamma(111) < \gamma(110) < \gamma(100)$ [50]. For clean Si surfaces the situation is slightly different and it was shown that the order is $\gamma(111) < \gamma(100) < \gamma(110)$. However, these surface energy relationships cannot solely predict the cross-section as the minimization of the surface-to-volume ratio must also be considered [50]. Zhang *et al* found the $\langle 112 \rangle$ nanowire to be defined by a single rectangle cross-section consisting of two (111) and two (110) facets which

has also been confirmed experimentally [55]. The $\langle 112 \rangle$ nanowires then have a practical advantage over the $\langle 110 \rangle$, $\langle 111 \rangle$ and $\langle 100 \rangle$ nanowires which can take on many different cross-section configurations based on low-index planes and may be difficult to selectively control and may lead to varying electrical and optical properties [102]. Unfortunately, the band structure for $\langle 112 \rangle$ Si nanowires is such that the band gap remains indirect even at extremely small diameters [103], whereas $\langle 110 \rangle$, $\langle 111 \rangle$ and $\langle 100 \rangle$ all have a crossover point from indirect to direct band gap when the diameter approaches a few nanometers in size [104]. Because of this, $\langle 112 \rangle$ Si nanowires may have limited use for photonic applications (although a few recent papers theoretically demonstrate the possibility of direct band gap $\langle 112 \rangle$ Si nanowires [105, 106]). Furthermore, $\langle 112 \rangle$ Si nanowires are more abundant when using the OAG method and difficult to controllably grow using the VLS method. Therefore, the choice of the Si nanowire growth direction needs to be a compromise between the available growth method, required nanowire size, material properties and applications.

Diameter-dependent directions were also observed for Au-catalyzed ZnSe nanowires epitaxially grown on GaAs substrates (figure 3) [107–109]. ZnSe nanowires larger than 20 nm preferred the $\langle 111 \rangle$ (figure 3(a)) direction whereas nanowires with smaller diameter preferred either the $\langle 110 \rangle$ (figure 3(b)) or $\langle 112 \rangle$ (figure 3(c)) direction. Vertical growth of $\langle 110 \rangle$ ZnSe nanowires on GaAs (110) was also demonstrated. Interestingly, for all three orientations, the interface between the ZnSe and the Au catalyst was either a single (111) plane or a multi-faceted surface consisting of several (111) and (001) surfaces which are thought to be the two lowest energy surfaces for ZnSe (figure 3(d)–(f)) [107].

The relationship between the growth direction and the nanowire diameter has also been shown to be dependent upon the catalyst material, most likely a result of the modification of the eutectic composition and nanowire-catalyst free surface energy [55, 100, 110]. Plasma excitation used in conjunction with CVD was found to improve the yield of $\langle 110 \rangle$ Si nanowires on a Si (001) substrate [111]. This was attributed to the shorter nucleation time from the increased cracking efficiency of SiH_4 with plasma excitation. Without plasma excitation, the polydisperse Au nanoparticles have ample time to coalesce and form larger nanoparticles (i.e. >20 nm) and seed nanowire growth in the $\langle 111 \rangle$ direction.

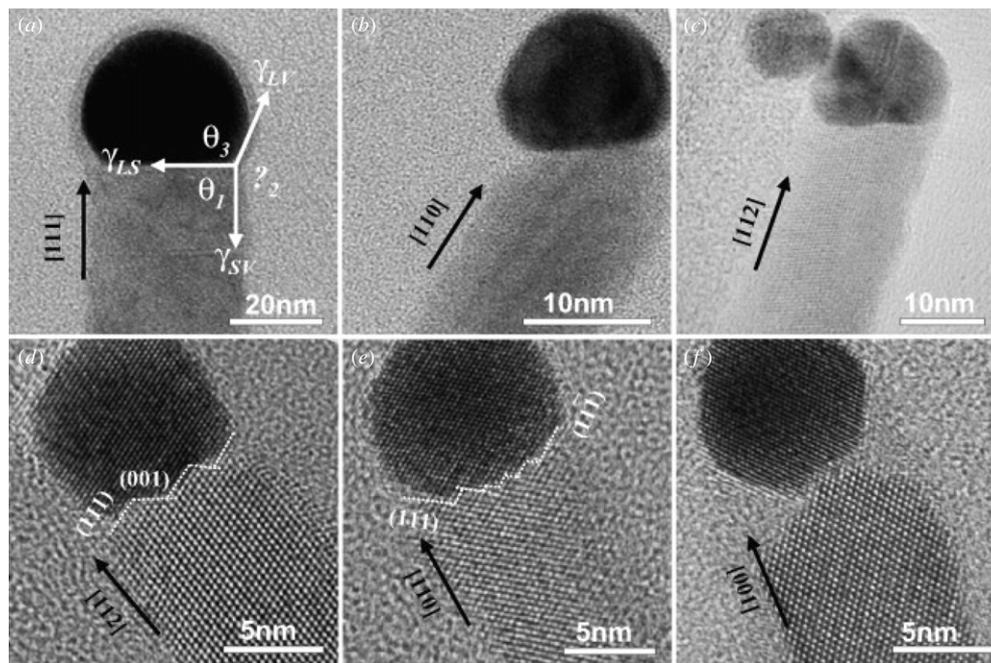


Figure 3. TEM images of ZnSe nanowires grown along (a) $\langle 111 \rangle$, (b) and (e) $\langle 110 \rangle$, (c) and (d) $\langle 112 \rangle$ and (f) $\langle 001 \rangle$ directions. In all cases, the interface between the Au and ZnSe nanowire is either a single (111) surface (a)–(c) or a combination of the lowest energy (111) and (001) surfaces (d)–(f). Adapted from [107] with permission.

2.4. Modification of orientation through growth conditions

The use of growth conditions as an *in situ* method of modifying nanowire orientation is an attractive and simple approach. By growth conditions we are primarily referring to growth temperature, pressure (total or partial pressure of precursors) and precursor molar ratios (e.g. group V/III). It should be emphasized that the growth conditions are not necessarily independent of each other. For example, a modification of the growth temperature may also result in a change of the effective precursor molar ratios in the case of MOCVD. Furthermore, the growth conditions may not be equivalent across the various growth apparatus used by different research groups. Growth temperature, for example, is not a directly measured parameter and is often instead measured indirectly from the susceptor or sample holder. These considerations must be kept in mind when interpreting results from the research community.

It was observed early on the importance of maintaining the stability of the catalyst and nanowire–catalyst interface through isothermal growth techniques in order to avoid kinking or any other unwanted features. Wagner *et al* used a nonisothermal growth technique to form a lateral temperature gradient across a (rather large) Si nanowire which modified the nanowire–catalyst interface morphology and induced kinking of a $\langle 111 \rangle$ nanowire to another $\langle 111 \rangle$ direction [9]. A study by Westwater *et al* clearly showed that it was possible to grow kink-free, straight Si nanowires only under a certain range of SiH_4 pressure and temperature conditions [51]. Underlining the importance of growth conditions, Ge *et al* observed a dependence on Si nanowire orientation when performing successive growths in a CVD reactor without cleaning the chamber between growths [112]. This was thought to be related to an increase of SiCl_4 in the growth zone as less

silicon was deposited on the sidewall of the quartz reactor. Similarly, Dick *et al* found that trace amounts of In remaining on the inner walls of an MOCVD reactor liner tube could affect subsequent nanowire growths even after the liner tube was thoroughly cleaned [90]. Considering these studies, the diversity of reported results for nanowire growth from the research community is not surprising. In addition, they highlighted the importance of rigorous experimental design to limit the memory effect of prior growths on experiments.

2.4.1. Temperature. The modulation of nanowire orientation through growth temperature change has been reported by several groups. Shan *et al* found that temperature controlled the preferred growth direction of wurtzite CdSe nanowires grown on GaAs substrates using MOCVD [113]. When grown at 480°C , most CdSe nanowires grew along the substrate $\langle 110 \rangle$ direction whereas at a higher temperature of 500°C the nanowires preferred the $\langle 111 \rangle$ direction, in both cases irrespective of the substrate orientation. Using MOCVD, we found that when GaAs nanowires were grown on (001) GaAs substrates at low temperature ($\sim 420^\circ\text{C}$) the $\langle 111 \rangle$ direction is preferred [58]. At higher temperatures ($>450^\circ\text{C}$) the majority of GaAs nanowires instead grew in the plane of the substrate in one of two $\langle 110 \rangle$ directions; this will be discussed in more detail in section 3. Ihn *et al* found an ideal growth temperature range of $530^\circ\text{C} \leq T \leq 580^\circ\text{C}$ for GaAs nanowire growth on (001) Si substrates using MBE [81]. Below 530°C , the GaAs nanowires were not epitaxially grown and thus oriented randomly with respect to the Si substrate. Cai *et al* reported on the temperature-dependent growth of ZnSe using MBE. Ultrathin ZnSe nanowires (~ 10 nm diameter) grew in a $\langle 110 \rangle$ direction when grown at 530°C but in the

$\langle 111 \rangle$ direction with a lower growth temperature of 390 °C. To explain the results, Cai *et al* modeled the nanowire as a column containing a solid nanowire, liquid-solid melt region, and liquid catalyst. Although the nanowire growth may initiate in the $\langle 111 \rangle$ direction, within the liquid-solid (LS) region atoms are mobile and can rearrange to modify the nanowire growth direction $\langle 110 \rangle$ or $\langle 112 \rangle$ to minimize energy as the nanowire grows provided the temperature is high enough such that the LS region is reasonably thick. At low temperatures, the LS region is insufficiently thick for a direction change and the nanowire may remain $\langle 111 \rangle$ even though it is of higher energy. Schmid *et al* found that when using CVD and SiH_4 , the highest yield of vertical epitaxial Si $\langle 111 \rangle$ nanowires on the (111) Si substrate occurred at $T < 470$ °C with yield decreasing with increasing temperature (shown graphically in figure 4(d)). Hanrath *et al* pointed out that Ge nanowires favor growth in the $\langle 111 \rangle$ direction when a high temperature growth process is used such as physical vapor transport (PVT) or laser catalyzed processes, whereas the $\langle 110 \rangle$ direction is preferred when Ge nanowires are grown at lower temperatures for example by preparing Ge nanowires in solution [56]. Clearly, growth temperature can modify the metal–semiconductor interface and thus the growth direction of the nanowire. However, the observed temperature effect for various semiconductor materials (CdSe, GaAs, Si, Ge, etc) using different growth methods (MOCVD, MBE, PVT, etc) reported by different groups does not seem to show a definitive preference of $\langle 111 \rangle$ versus non- $\langle 111 \rangle$ in the high or low-temperature regime. This is probably because of the differences in other growth parameters under the reported growth conditions, and underscores the interconnection between temperature and other growth parameters.

2.4.2. Total pressure and precursor partial pressure. Huyn and Lugstein *et al* recently demonstrated a controllable way of changing the growth direction of Si nanowires between the $\langle 111 \rangle$ and $\langle 112 \rangle$ directions by modifying the total pressure of a CVD chamber [54, 115]. Using the SiH_4 precursor and Au catalyst they found that at a total reactor pressure of 3 mbar the Si nanowires preferred to grow in a $\langle 111 \rangle$ direction (figure 5(a)). After increasing the total pressure to 15 mbar while maintaining the same SiH_4 flow rate, the nanowires were then found to predominantly grow along a $\langle 112 \rangle$ direction (figure 5(b)). They demonstrated that it was possible to switch between orientations on the same nanowire simply by modifying the total pressure (figure 5(c)). In this manner, kinking of the nanowires can be controlled [115]. The mechanism behind the orientation change is not completely clear. TEM does not show any defects at the kinking site of a nanowire that changed from a $\langle 111 \rangle$ to $\langle 112 \rangle$ growth direction and therefore the orientation change is likely driven instead by the energetics of the nanowire and the amount of Si available in the reactor, or the growth rate enhancement by more than an order of magnitude (figure 5(c)) as a result of the pressure increase.

Schmid *et al* found that a growth direction change was possible for epitaxial Si nanowires grown on Si $\langle 111 \rangle$ substrates when they maintained a constant CVD total reactor

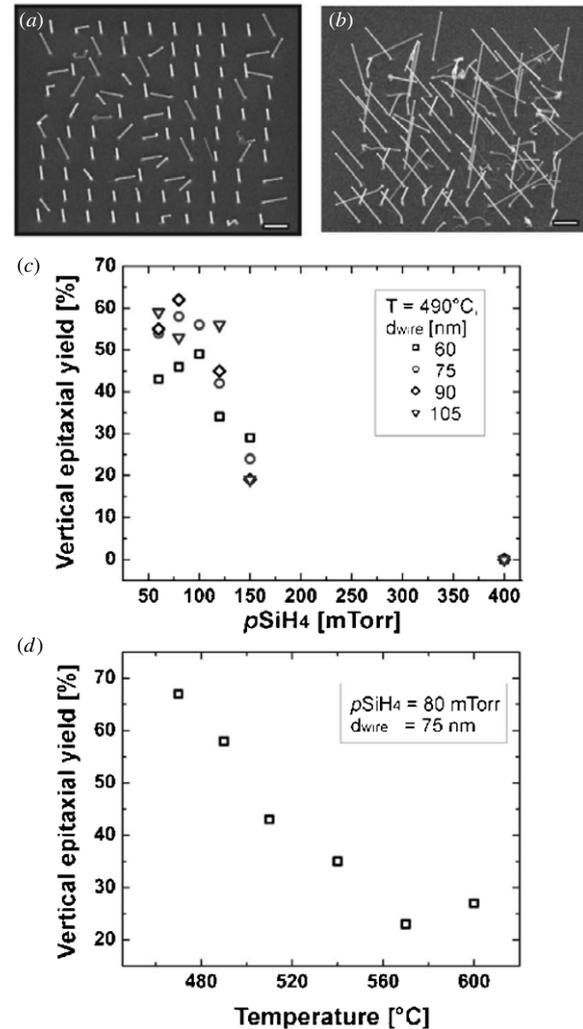


Figure 4. Effect of precursor partial pressure and growth temperature on the epitaxial silicon nanowire growth direction. (a) Array of silicon nanowires grown with SiH_4 partial pressure of 80 mTorr. Most nanowires grow in the vertical $\langle 111 \rangle$ direction. (b) Array of silicon nanowires grown with the SiH_4 partial pressure of 400 mTorr. Nanowire kinking is widely observed. (c) Yield of vertical epitaxial wires as a function of partial pressure for several nanowire diameters. (d) Yield of vertical epitaxial wires as a function of temperature for 75 nm diameter silicon nanowires. Adapted from [114] with permission.

pressure but modified the partial pressure of SiH_4 (figure 4) [114]. At low SiH_4 partial pressure (< 150 mTorr), Si nanowires tend to grow in the vertical $\langle 111 \rangle$ direction (figure 4(a)). At higher SiH_4 partial pressure, yield of vertical $\langle 111 \rangle$ nanowires decreases and instead the nanowires prefer to grow toward the other available out-of-plane $\langle 111 \rangle$ directions (figure 4(b)). Westwater *et al* reported similar results [51]. Jagannathan *et al* showed that the ratio of vertical $\langle 111 \rangle$ to non-vertical $\langle 111 \rangle$ Ge nanowires grown on (111) was inversely proportional to GeH_4 partial pressure when it was increased from 0.275 to 1.8 Torr [80].

For III–V materials, the ratio between the molar flow rates of the group-V and group-III precursors (V/III ratio) can significantly influence the growth rate and morphology of III–V nanowires [116–119]. Kinking and non- $\langle 111 \rangle$ growth

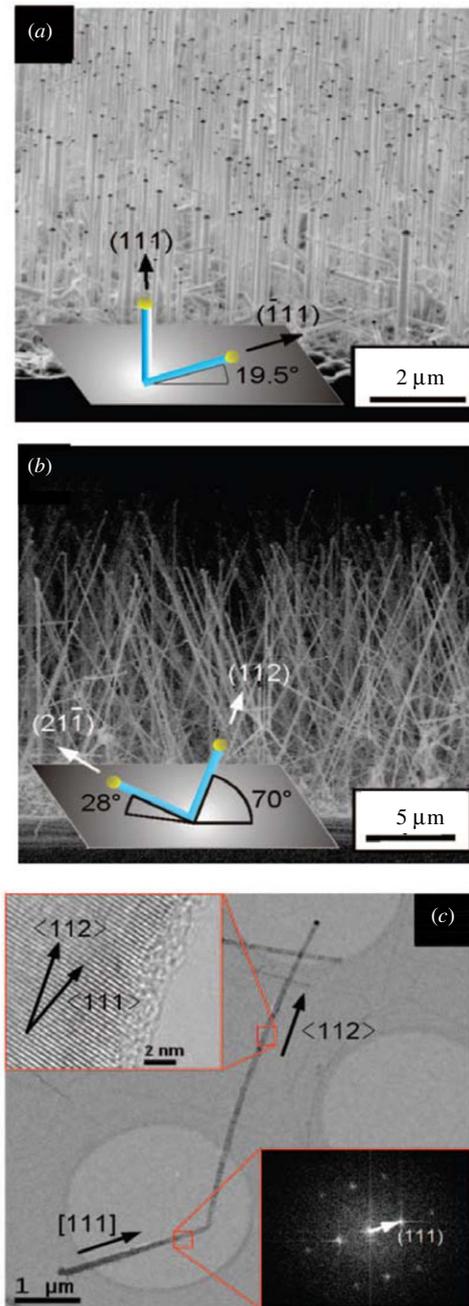


Figure 5. Pressure induced orientation change of silicon nanowires. (a), (b) Side view SEM images of Si nanowires where (a) $\langle 111 \rangle$ nanowires were grown for 100 min at 500 °C with a total pressure of 3 mbar and (b) $\langle 112 \rangle$ nanowires were grown for 60 min at 500 °C with a total pressure of 15 mbar. (c) The growth direction of a single Si nanowire is modified by dynamically changing the total pressure. The nanowire was first grown at 3 mbar for 70 min and then at 15 mbar for an additional 30 min. Adapted from [54] with permission.

directions were observed for GaAs nanowires when a V/III ratio >90 was used with AsH_3 and trimethylgallium (TMG) precursors [119]. Joyce *et al* suggested the possibility of stable As trimers forming on the $\langle 111 \rangle_B$ surface with a high V/III ratio that may modify the surface energetics and allow for other growth directions. The high V/III ratio may also hinder Ga diffusion into the Au particle which could modify the GaAs-Au eutectic and hence the growth direction. Temperature

variations across the growth substrate will cause the V/III ratio to vary locally potentially resulting in edge effects [117]. Furthermore, some studies have shown the pyrolysis rate of the group-V precursors AsH_3 and PH_3 is enhanced by the Au catalyst on the growth surface resulting in a local V/III ratio dependent upon the catalyst density when these particular hydrides were used [116, 120].

3. In-plane nanowire growth

Nanowires are generally grown in a direction that is vertical or angled from a growth substrate. As we discussed in the introduction this geometry has been used with great success, although there are distinct advantages to growing nanowires in a direction parallel and in-plane with the growth surface. For example, the vertical type geometry (e.g. $\langle 111 \rangle$ nanowires grown on a $\langle 111 \rangle$ substrate) results in a high aspect ratio that complicates device fabrication and requires advanced processing techniques. Nanowires grown in-plane with the growth surface are more suitable for conventional planar processing techniques. There are generally two approaches to in-plane nanowire growth: (1) grow nanowires from etched facets (such as sidewalls and V-grooves) on the substrate surface and (2) grow nanowires in the plane of the substrate surface under unconventional growth conditions. The first approach was initially demonstrated using GaAs [121] but has been more widely used for Si [122–125]. On the Si $\langle 110 \rangle$ substrate, deep trenches with $\langle 111 \rangle$ sidewalls can be easily formed with an anisotropic etch. Au nanoparticles can then be deposited and $\langle 111 \rangle$ Si nanowires can nucleate on one $\langle 111 \rangle$ sidewall and bridge over to the adjacent sidewall. A similar approach can be used for other materials systems [126–131]. Further discussion of this technique is beyond the scope of this paper; instead we refer the reader to the several aforementioned references. Here, we focus on the second approach and the possibility of growing nanowires in an unconventional direction that is in-plane with the growth substrate.

Planar-like ‘crawling’ ZnO nanowires have been commonly observed on sapphire and GaN substrate surfaces mixed with other ZnO nanowire vertical growth modes [68, 69, 134–136]. These crawling ZnO nanowires are generally observed to be root-like and grow in a random direction without clear crystallographic relationship with the underlying substrate, have poor crystallinity [134] and are thus generally considered to be a nuisance, for example, when interpreting photoluminescence emission spectra. Wang *et al* found that crawling ZnO nanowire growth was suppressed when $\text{Al}_x\text{Ga}_{1-x}\text{N}$ substrates were used [137]. Fan *et al* reported that crawling growth was more prevalent with increased temperature and larger Au catalyst size when growing ZnO nanowires on (0001) GaN with CVD, suggesting that diffusion of Au from the primary Au particle was catalyzing the crawling growth [138]. By confining ZnO nanowire growth within parallel cracks on the GaN surface, Fan *et al* demonstrated the growth of aligned ZnO nanowalls [138] through interconnected crawling ZnO nanowires similar to

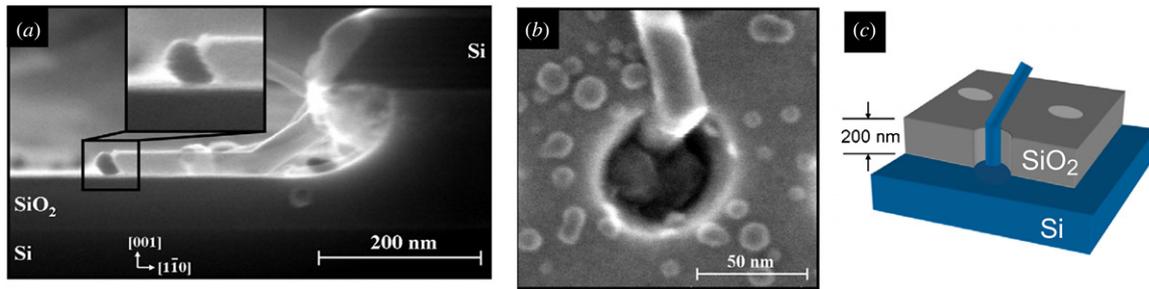


Figure 6. Guided growth of Si nanowires using SiO₂. (a): $\langle 111 \rangle$ Si nanowire grown from a Si etched ledge abruptly changes growth direction to $\langle 110 \rangle$ when it comes in contact with the buried oxide (BOX) of a SOI wafer [132]. (b) and (c): SEM image and schematic illustration showing a Si nanowire guided in the $[001]$ direction abruptly turns to the $\langle 111 \rangle$ direction above the BOX. Adapted from [133] with permission.

randomly aligned ZnO nanowalls reported by other groups [139, 140].

Nikoobakht *et al* demonstrated the growth of well-aligned planar ZnO nanowires on *a*-plane sapphire substrate using a phase transport process and Au catalyst [141, 70]. The growth axis of the planar ZnO nanowires was along the $\pm [1-100]$ directions which are also parallel with the $[1-100]$ direction of the sapphire substrate suggesting an epitaxial relationship between the nanowire and substrate. As described above, the *a*-plane sapphire and *c*-plane of ZnO are very closely lattice matched; thus, such planar ZnO nanowires should grow relatively strain-free on the *a*-plane sapphire surface. Field-effect devices were fabricated utilizing the self-registration property of planar ZnO nanowires that were first grown laterally from a pre-defined Au pad. For Au catalyst sizes larger than about 20 nm it was observed that the planar ZnO nanowires lose their crystallographic alignment or grow out of the plane of the substrate which indicates that the presence of increased strain may preclude the possibility of larger sized ZnO nanowires to grow laterally in an aligned manner.

Quitoriano and co-workers have recently reported a novel method of engineering the growth of Si nanowires in the $\langle 110 \rangle$ direction through the use of a SiO₂ guiding layer (figure 6) [132, 133]. A KOH etch was used to etch the top Si layer of a SOI Si (001) substrate and expose the underlying buried oxide (BOX). The top Si layer was further undercut by etching the BOX thus forming Si ledges overhanging a trench. Au nanoparticles were deposited and used to nucleate nanowire growth on the Si ledges. Surprisingly, nanowires that grew in a $\langle 111 \rangle$ toward the BOX were forced into a $\langle 110 \rangle$ growth direction when the nanowires came in contact with the BOX (figure 6(a)). The interface between the Au and Si remained a single $\langle 111 \rangle$ plane. The nanowires then continued to grow in a $\langle 110 \rangle$ direction on top of the BOX until the adjacent ledge was reached. It was possible to connect two electrodes in this manner with a $\langle 110 \rangle$ bridging nanowire and form an isolated FET device. Quitoriano *et al* further extended this SiO₂ guiding technique by patterning Au within small oxide windows on a Si (001) substrate. They found that it was possible to grow the Si nanowires vertically through the oxide windows in an otherwise generally energetically unfavorable vertical $\langle 001 \rangle$ direction (figures 6(b)–(c)) [133].

There have been a handful of reports of III–V nanowires growing on the surface of the (001) and $\langle 111 \rangle$ B substrate;

typically terminating at the base of a $\langle 111 \rangle$ B nanowire [14, 29, 57–59, 64, 66, 93]. III–V nanowires will sometimes begin by growing on the (001) surface in the $[1-10]$ or $[-110]$ direction for a few hundreds of nanometers before abruptly changing orientation to the more typical $\langle 111 \rangle$ B direction. Mikkelsen *et al* comprehensively studied this planar nanowire growth using scanning tunneling microscopy (STM) and found the nanowires to have an epitaxial relationship with the (001) substrate [57]. Not surprisingly then, a PLL functionalized surface will block the planar nanowire growth [93]. Zhang *et al* observed planar growth of InAs nanowires with the Au catalyst on the GaAs $\langle 111 \rangle$ B surface. The growth of these planar InAs nanowires occurred such that the Au catalyst maintained a $\{111\}$ interface with the InAs nanowire and a $\langle 111 \rangle$ B interface with the GaAs surface and thus the nanowires grew in the six $\langle 112 \rangle$ directions available in the plane of the substrate surface [66].

We recently demonstrated controlled growth of such planar $\langle 110 \rangle$ GaAs nanowires on a GaAs (001) surface using the atmospheric pressure MOCVD and Au catalyst (figure 7) [29, 58]. We found that at low growth temperature ($<450^\circ\text{C}$) GaAs nanowires preferred to grow in the $\langle 111 \rangle$ B direction whereas at higher growth temperatures ($>450^\circ\text{C}$) planar $\langle 110 \rangle$ nanowire growth was preferred (figures 7(a)–(b)). TEM confirmed that the self-aligned planar $\langle 110 \rangle$ nanowires are zinc-blende, mostly free of stacking faults, and have an epitaxial relationship with the (001) surface (figure 7(c)). We have proved that the planar $\langle 110 \rangle$ nanowire growth does not depend on a nanowire diameter and does not seem to change within a large range of V/III ratio (36 – 90). Using an n-type planar $\langle 110 \rangle$ GaAs nanowire ($N_d = 2.3 \cdot 10^{17} \text{ cm}^{-3}$) as the channel material of a metal-semiconductor field effect transistor (MESFET), we extracted a bulklike electron mobility of $4120 \text{ cm}^2 (\text{V s})^{-1}$ from electrical measurements at room temperature and confirmed the extremely high material quality of the planar GaAs nanowires [29]. Planar $\langle 110 \rangle$ GaAs nanowires can also be transferred to other substrates such as Si by growing them first on a sacrificial layer (e.g. $\text{Al}_x\text{Ga}_{1-x}\text{As}$) that is then selectively removed with a wet etch to release the planar nanowires from the GaAs growth substrate [58]. A polydimethylsiloxane (PDMS) stamp can then be used to pick and place the released planar nanowires onto another substrate. Shown

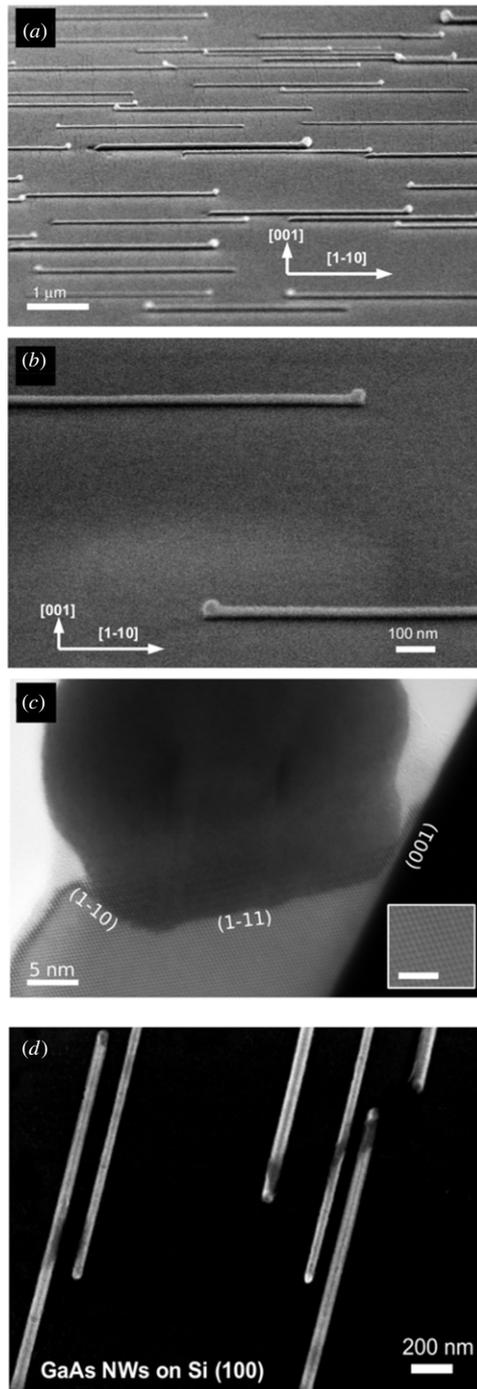


Figure 7. Planar $\langle 110 \rangle$ GaAs nanowires on the (001) GaAs substrate grown with MOCVD. (a), (b) Tilt SEM view of planar $\langle 110 \rangle$ nanowires are (a) highly aligned along the anti-parallel $\langle 110 \rangle$ directions with (b) the uniform diameter and smooth morphology. Larger diameter nanowires show trapezoidal cross-section. (c) TEM confirms that the planar GaAs nanowires are zinc-blende, mostly free of stacking faults, and have an epitaxial relationship with the substrate. The interface between the Au catalyst is multi-faceted with a large (111) surface and two smaller (001) and $(1-10)$ surfaces. The inset scale bar is 2.5 nm. (d) $\langle 110 \rangle$ GaAs nanowires transferred to a silicon substrate while maintaining position and alignment. Adapted from [58] with permission.

in figure 7(d) are planar $\langle 110 \rangle$ GaAs nanowires that were transferred to a silicon substrate; clearly, the global and local

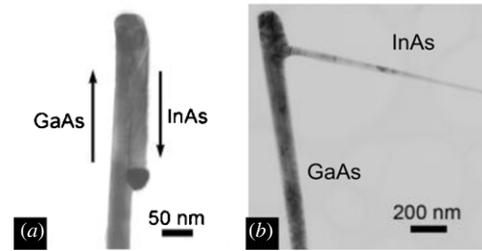


Figure 8. TEM images of kinked GaAs/InAs nanowires with different InAs segment growth times. (a) The InAs portion of the nanowire grows back over the top of the original GaAs nanowire. (b) The InAs segment kinks outward from the original nanowire when a region of InAs overgrowth is reached. Adapted from [143] and [144] with permission.

positioning and alignment were maintained after the nanowires were transferred. With further development, this technique holds promise as a wafer-scale method of obtaining position-controlled and aligned nanoscale III–V materials on silicon and other substrates.

4. Nanowire kinking and branching

Kinking or branching is the abrupt change in the growth direction of a nanowire and is usually a random and thus deleterious effect. However, control over the kink location and kinking direction will allow for sophisticated 3d nanowire structures with interesting applications. Growth conditions (in particular, temperature and precursor partial pressures) can be used to induce nanowire kinking. Wagner *et al* found that abrupt temperature changes affect the stability of the nanowire-catalyst eutectic and will cause a kink [9]. It has been suggested that stacking fault defects in III–V nanowires may act as a kinking site [64]; however, others have reported no relationship between stacking faults and kinking [119].

By changing the composition of the nanowire during growth through insertion of an axial heterojunction, it is possible to control the position of a kink. Dick *et al* studied [142] several different combinations of group-IV and III–V materials and found that the growth behavior when the material composition is changed can be classified as one of two possible outcomes: (1) the nanowire continues to grow in the same direction and will remain straight (2) the nanowire will kink or grow backward on top of itself (e.g. figure 8(a)). Surprisingly, the outcome was dependent upon which material was grown first. For example, the growth of GaP on a Si nanowire will result in a straight nanowire whereas the growth of Si on a GaP nanowire causes a kink. Dick *et al* hypothesized the kinking occurs when island growth (Volmer-Weber) occurs at the nanowire–catalyst interface rather than layer-by-layer growth (Frank-van der Merwe) which is less energetically favorable depending upon the composition of the nanowire and catalyst. *In situ* TEM of Ge grown on GaP shows that a Ge island initially precipitates at the three-phase boundary between the Au catalyst and GaP nanowire. As the nucleus grows the Au catalyst is pushed perpendicular to the original growth direction and eventually wraps around the original GaP nanowire and continues to travel down the nanowire sidewall.

Paladugu *et al* studied InAs grown on GaAs nanowires and noted that the Au catalyst prefers to maintain an interface with GaAs because of the lower surface free energy and thus drives the movement of the Au and growth of InAs down the original GaAs nanowire as shown in figure 8(a) [143]. In a later study, Paladugu *et al* showed that eventually this InAs segment will branch away from the nanowire once a region of considerable InAs radial overgrowth on the GaAs nanowire is reached (figure 8(b)) [144]. Lattice mismatch appears to have little importance in any of these studies. Indeed, the interface with the largest lattice mismatch (GaP grown on InAs) will result in a straight unknicked nanowire [142].

Treelike nanostructures, or nanotrees, can be formed by growing nanowire 'branches' from a single nanowire 'trunk' using the VLS mechanism [142, 145, 146]. Dick *et al* demonstrated the fabrication of GaP nanotrees by first growing vertical GaP trunks in the $\langle 111 \rangle_B$ direction on $(111)_B$ GaP substrates followed by deposition of Au onto the trunks and a second growth step to nucleate and grow the GaP branches from the main nanowire trunk. The GaP branches were epitaxially coherent with the trunk and grew in one of three possible $\langle 111 \rangle_B$ directions separated by 120° when viewed from above. Interestingly, another group of three $\langle 111 \rangle_B$ directions was possible if the branches nucleated on a rotationally twinned segment of the GaP trunk. A total of six $\langle 111 \rangle_B$ orientations directed outward from the trunk (each separated by 60°) was then possible. In a later study, Dick *et al* grew position-controlled nanotrees using InAs trunks and branches [146]. The trunks were aligned vertically in the $\langle 111 \rangle_B$ direction on a $(111)_B$ InP substrate whereas the branches grew in a $\langle 112 \rangle$ direction relative to the substrate. With proper positioning of the initial trunk, branches from adjacent trunks could connect forming nanotree networks. Wang *et al* reported the growth of non-epitaxial nanotree structures made from Si and GaN [145]. The Si branches were characterized with TEM and found to grow in a $\langle 111 \rangle$ direction with respect to the Si nanowire trunk.

5. Conclusion

In summary, we have reviewed and discussed various factors that affect the growth direction of VLS grown epitaxial semiconductor nanowires. This paper provided an indexed glimpse on the control of nanowire growth directions and thus the mechanical, electrical and optical properties associated with the crystal orientation.

The factors affecting the nanowire growth direction include substrate orientation, surface chemical treatment, nanowire diameter, metal initial catalyst–semiconductor eutectic composition, pre-growth annealing condition, growth temperature, pressure, precursor molar ratios, etc. Many of these factors are interconnected and the controllable parameter space to yield a certain growth direction is no doubt multi-dimensional. In principle, the resulting nanowire growth direction is dictated by the energetics of the nanowire surface facets and nanowire–catalyst interface, and the availability of nucleation sites and kinetic control. Of particular interest is the formation of in-plane nanowire growth investigated by a

number of groups, which has the potential to simplify the fabrication process and make large area planar processing for manufacturing of future nanowire array based electronic and photonic devices a reality. There is no doubt that more studies are needed to further elucidate the underlying mechanism for the control of orientations, including growth on offcut substrates and perturbation of the nucleation stage.

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